

BTQ00 Rev0.1 Schematics Document

Intel Prescott uFCPGA-478 / P4 Northwood

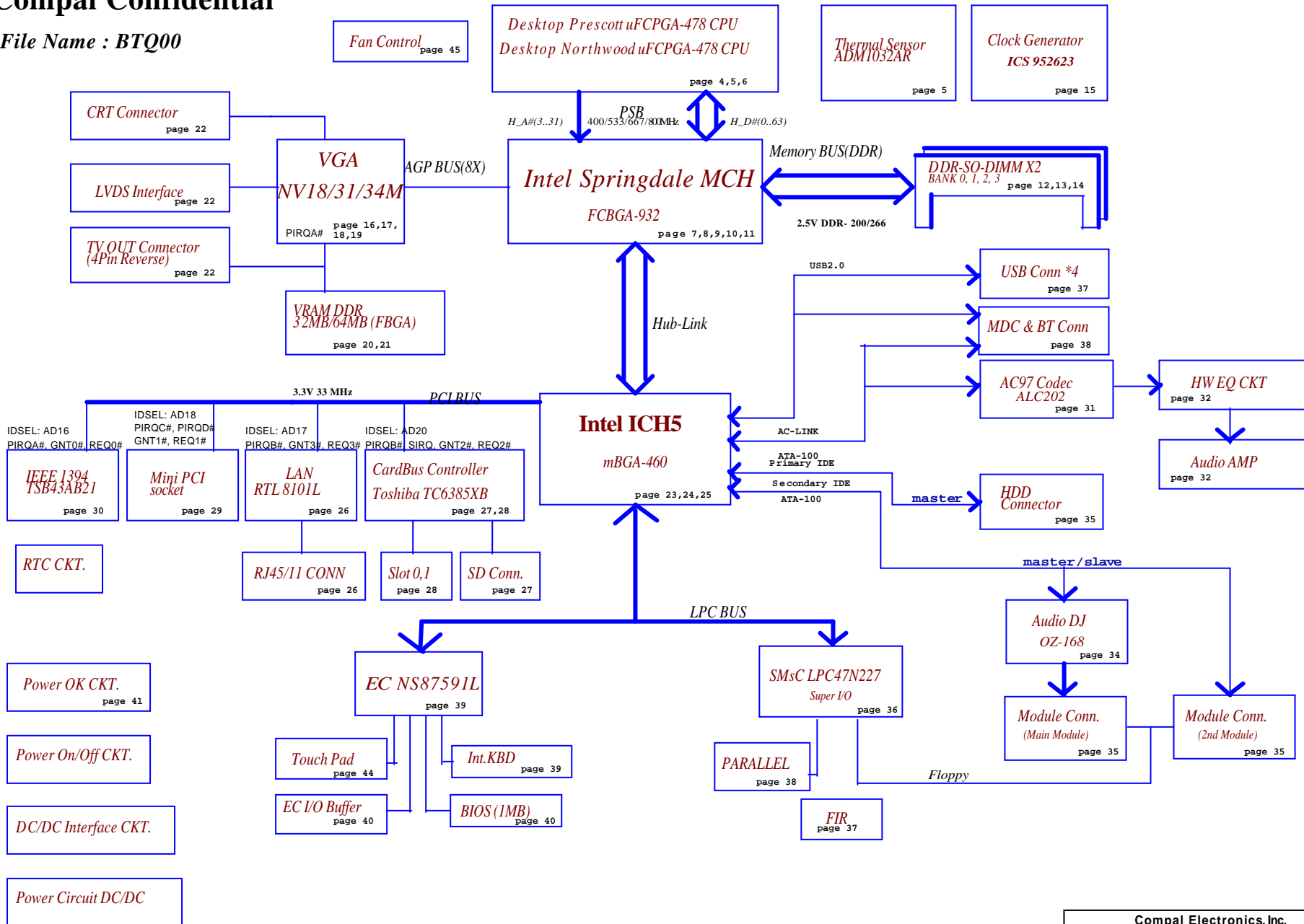
with Springdale / ICH5 / nVIDIA NV18/34/31M chipset

2003/02/20

Title		
Compal Electronics, Inc.		
Document Number		
Cover Sheet		
Size	Document Number	Rev
B	LA-1841	0.1
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Compal Confidential

File Name : BTQ00



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Block Diagram		
File		
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter powersupply(19V)	N/A	N/A	N/A
B+	AC or battery power rail for powercircuit	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+CPU_VID	1.2V switched power rail for CPU AGTL Bus	ON	OFF	OFF
+VTT_GMCH	+1.225V (Prescott) / +1.45V (Northwood)	ON	OFF	OFF
+VGA_CORE	1.2V switched power rail for VGA chip	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	AGP 4X/8X	ON	OFF	OFF
+2.5V	2.5V power rail	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+RTC_VCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#GNT#	Interrupts
VGA			PIRQA
CardBus	AD20	2	PIRQA/PIRQB
LAN	AD17	3	PIRQB
Mini-PCI	AD18	1/4	PIRQC/PIRQD
1394	AD16	0	PIRQA
SD	AD22		

EC SM Bus1 address

EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 110X b
EEPROM(24C1602)	1010 000X b	OZ168	0011 0100 b
(24C04)	1011 000Xb		

ICH4 SM Bus address

Device	Address
Clock Generator (ICS 952623)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM1	1001 001Xb

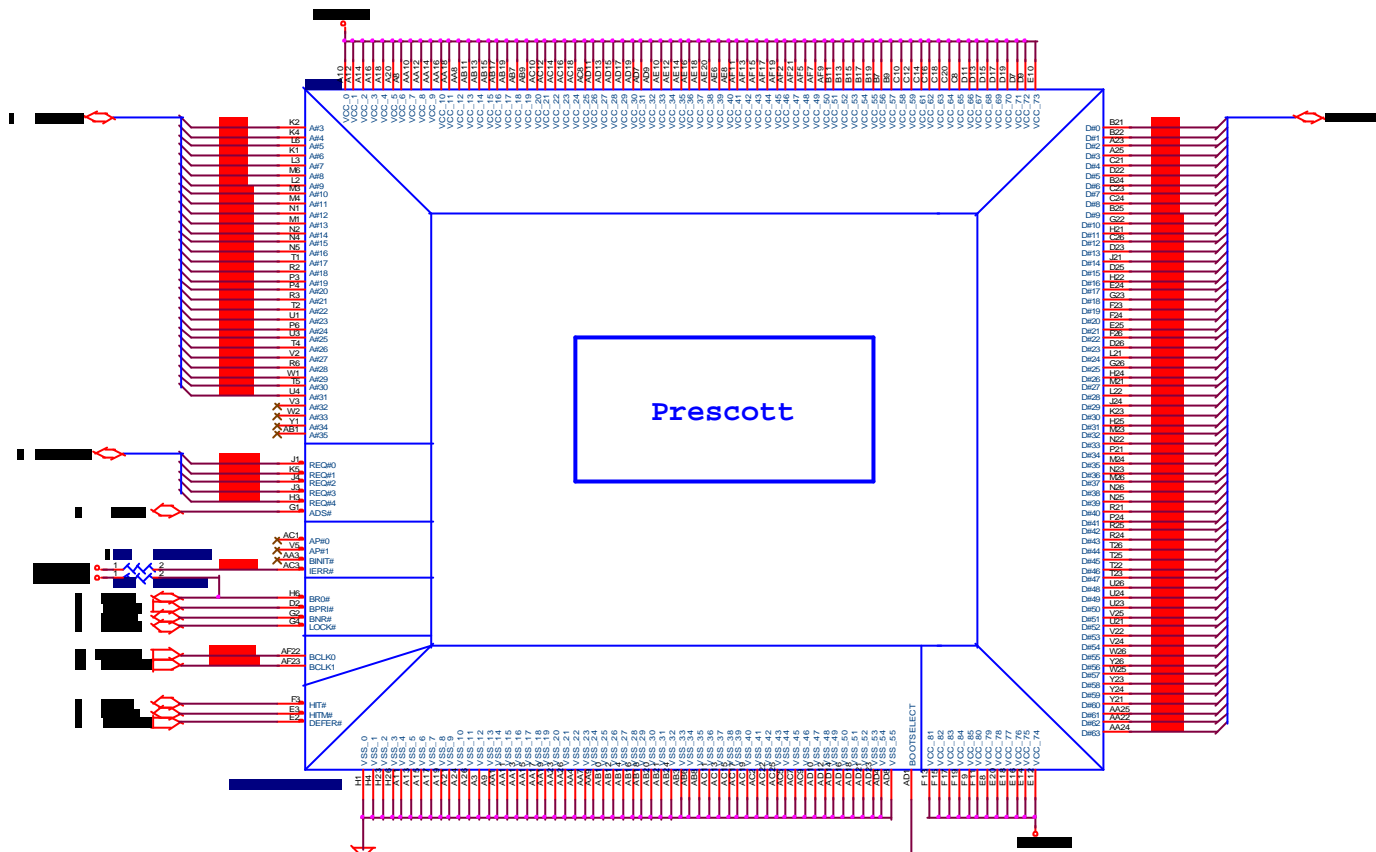
STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID_min	VAD_BID_typ	VAD_BID_max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

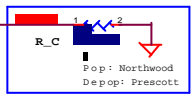
Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

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Notes		
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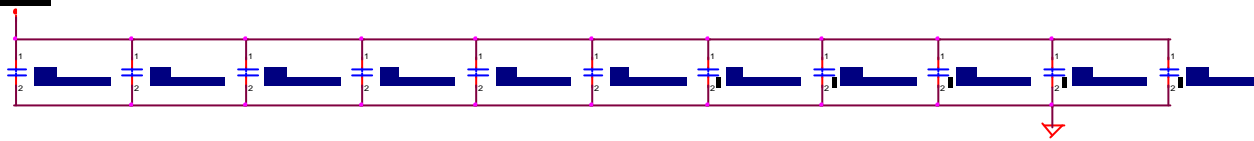
Reference Intel document
 Desktop P4 Spec.: 10988 P4 0.13u 512KB L2 EMTS Rev.2.0
 Desktop Prescott Spec.: 11910 Prescott EMTS Rev.0.5

Pin number	Northwood Pin name	Comment	Prescott Pin name	Comment	Northwood	Prescott
B6	FERR#	Pull-up 62ohm to +VCC_CORE	FERR#/PRE#	Pull-up 62ohm to +VCC_CORE	Pop	Pop
AA20	ITPCLKOUT0	Pull-up 56ohm to +VCC_CORE	TESTH16	Pull-up 62ohm to +VCC_CORE	Pop	Pop
AB22	ITPCLKOUT1	Pull-up 56ohm to +VCC_CORE	TESTH17	Pull-up 62ohm to +VCC_CORE	Pop	Pop
AD2	NC	float	VIDPWRGD	Pull-up 8.2kohm to +VCCVID	Depop	Pop
AD3	NC	float	VID5	Pull-up 1kohm to +3VRIN & connect to PWRIC	Depop	Pop
AF3	NC	float	VCCVIDL#	Connect to +VCCVID	Depop	Pop
AD20	VCCA	Connect to CPU Filter	VCCIOPLL	Connect to CPU Filter		
AF23	VCCIOPLL	Connect to CPU Filter	VCCA	Connect to CPU Filter		
AD1	VSS	Connect to GND	BOOTSELECT	CPU determine	Pop	Depop
AE26	VSS	Connect to GND	OPTIMIZED/COMPAT#	float	Pop	Depop



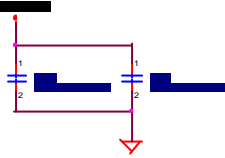
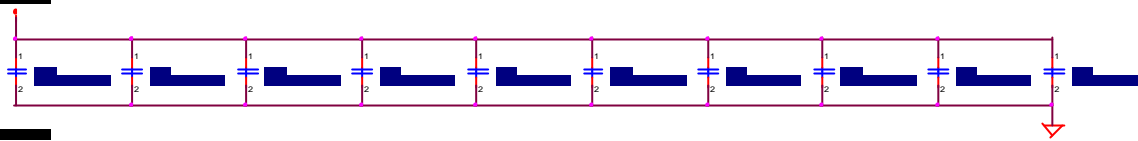
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 Prescott Processor in uFCPGA478 (1/2)
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Place 11 North of Socket(Stuff 8)

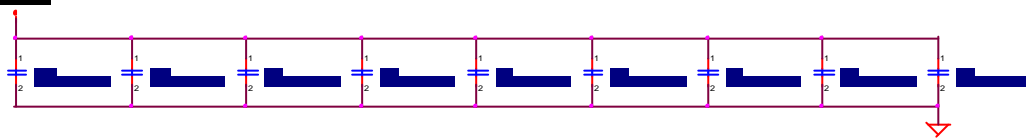


22uF depop reference
Springdale Customer Schematic R1.2 page82

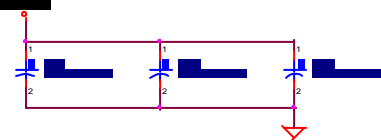
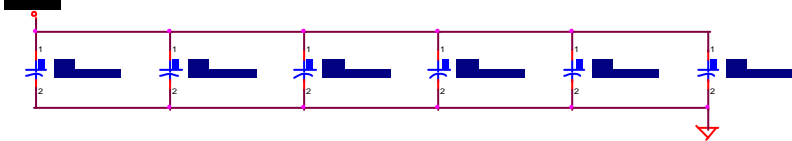
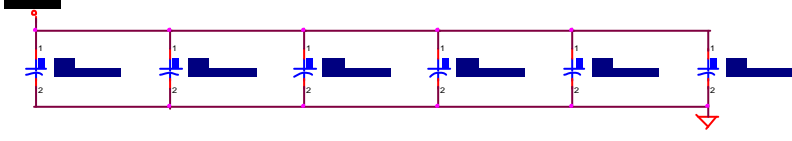
Place 12 Inside Socket(Stuff all)



Place 9 South of Socket(Unstuff all)



470uF _ERS10m ohm* 15, ESR=0.5m ohm



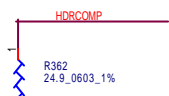
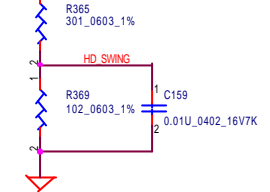
Decoupling Reference Document:
Springdale Chipset Platform Design guide Rev1.11
(12474)page239

Decoupling Reference Requirement:
560uF Polymer, ESR:5m ohm(each) * 10
22uF X5R * 32

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CPU Decoupling

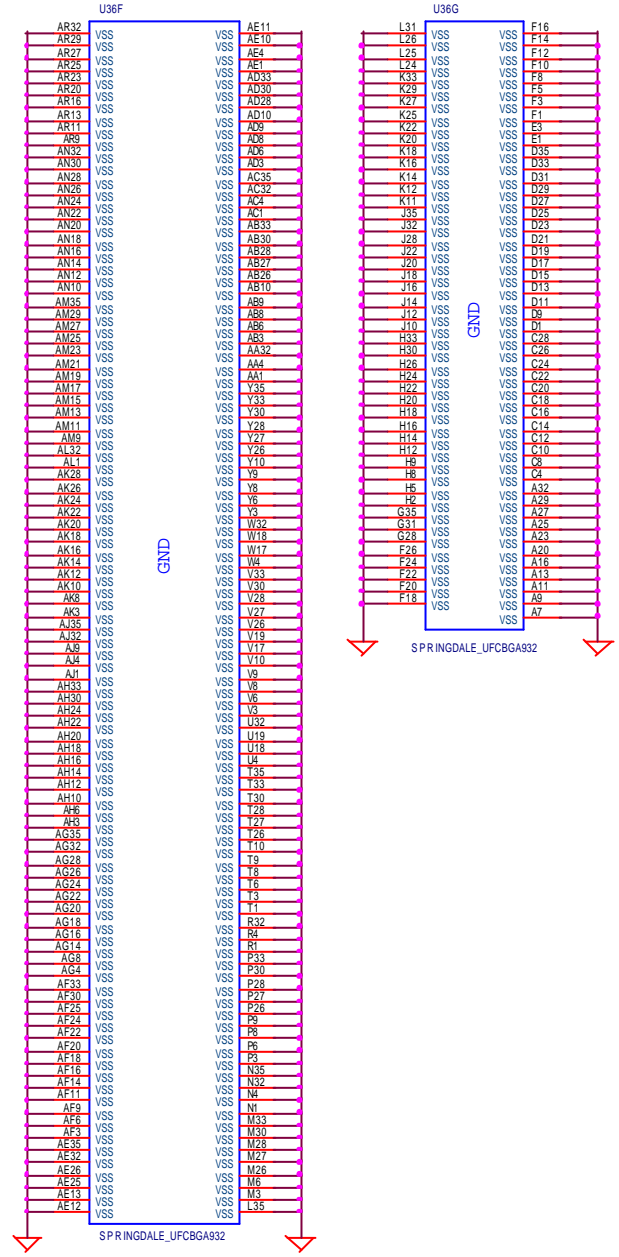
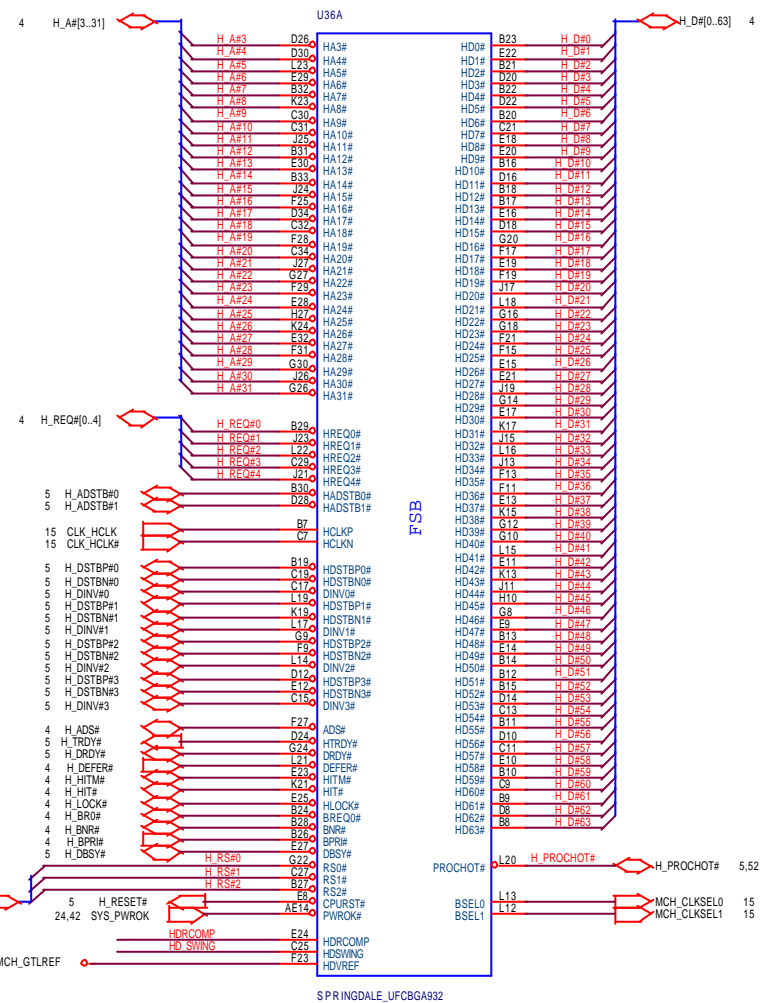
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Trace width 10mils, Space 7mils



GTL Reference Voltage Layout note:

- +GMCH_GTLREF Trace wide 12mils(min), Space 15mils.
- Place decoupling cap 220PF near GMCH.



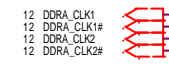
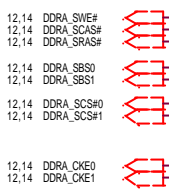
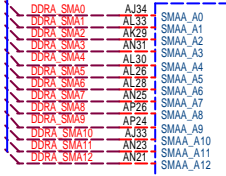
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Springdale-Host/GND (1/4)		
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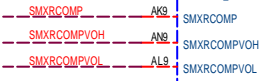
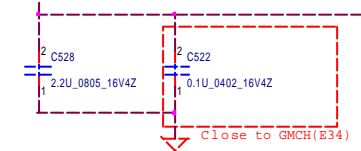
12,14 DDRA_SMA[0..12]

DDRA_SMA[0..12]

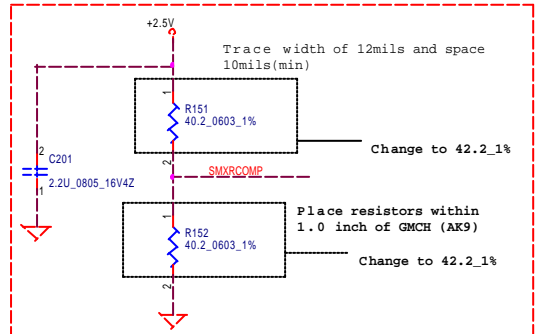
U36B



+SM_VREF_A +SM_VREF_A trace width of 12mils and space 12mils(min)

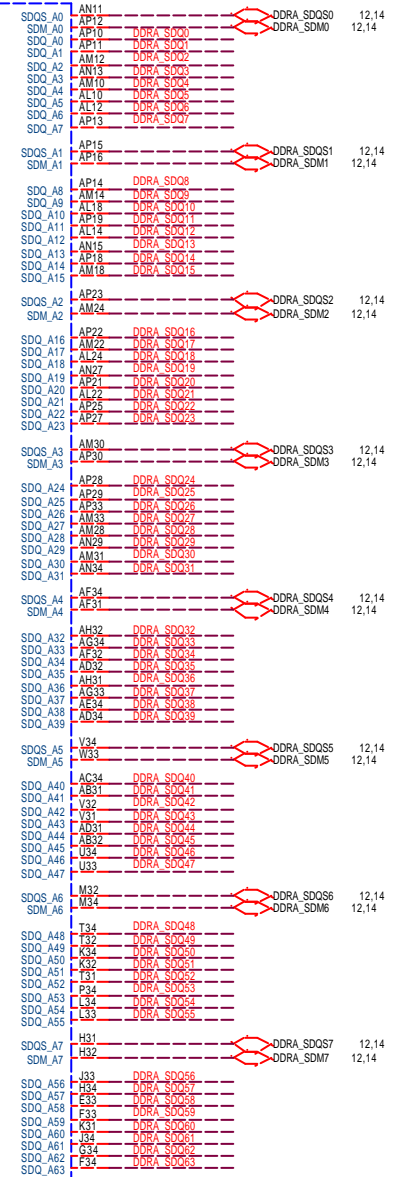


Close to GMCH(B34)



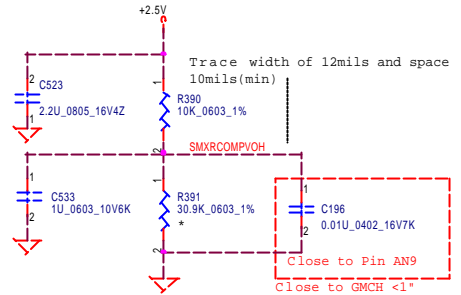
Change to 42.2.1% Place resistors within 1.0 inch of GMCH (AK9) Change to 42.2.1%

DDR Channel A

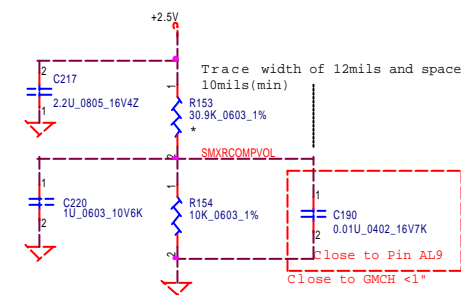


SPRINGDALE_UFCBGA832

DDRA_SDO[0..63] DDRA_SDO[0..63] 12,14

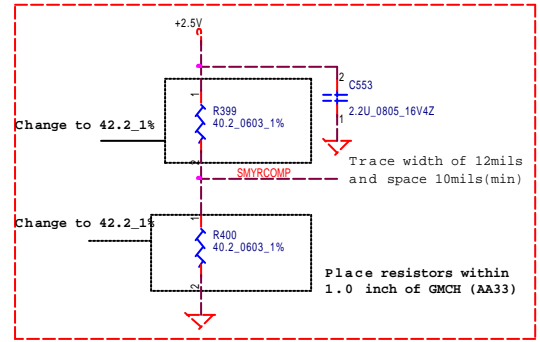
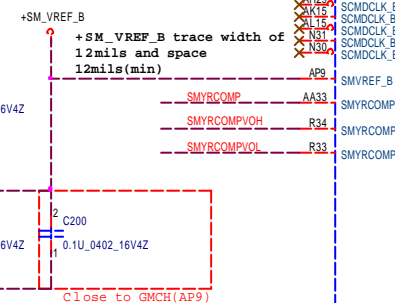
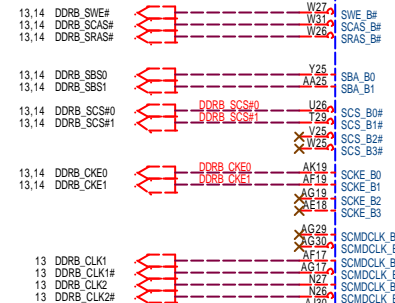
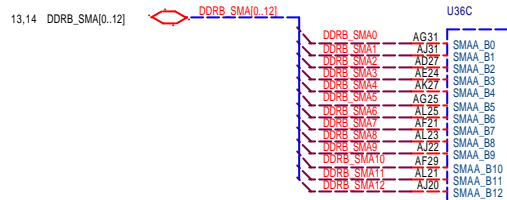


* Change to 31.12K Follow Intel design guide R1.1.1(12474) page124,125

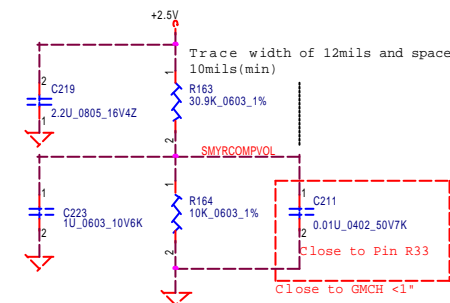
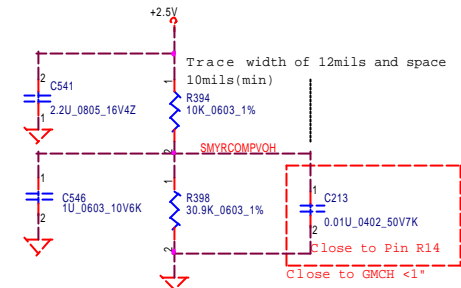
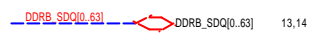
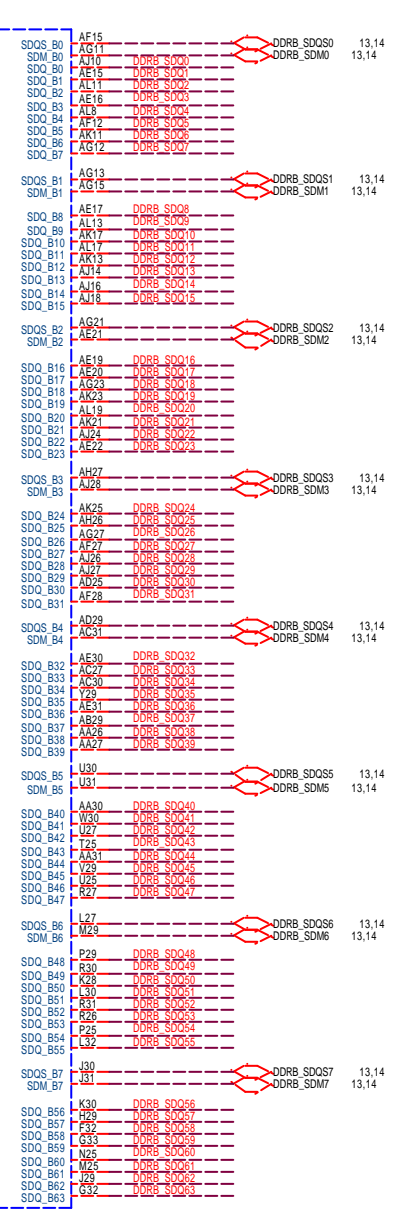


Compal Electronics, Inc.
 Springdale-DDR Interface-A(2/5)
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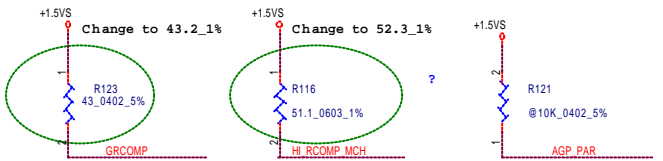


DDR Channel B

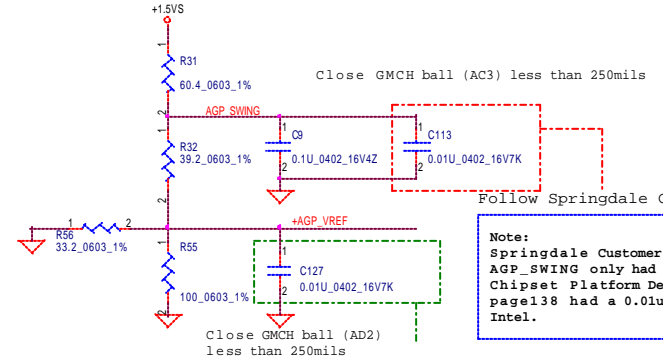
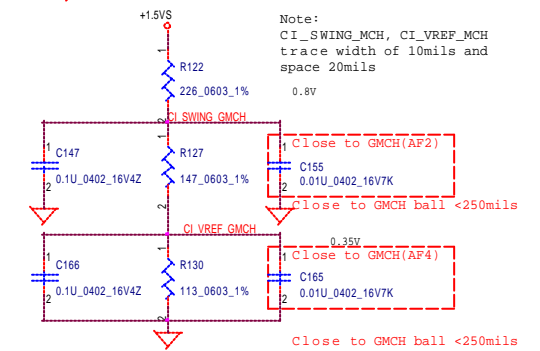
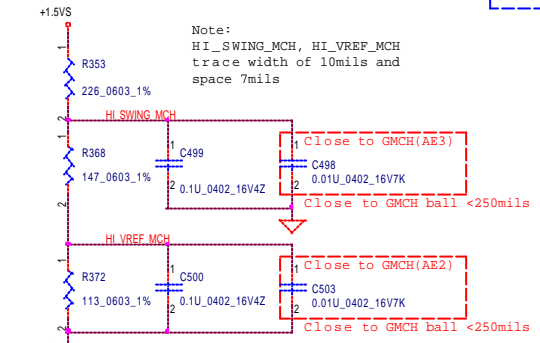


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Springdale-DDR Interface-B(3/5)			
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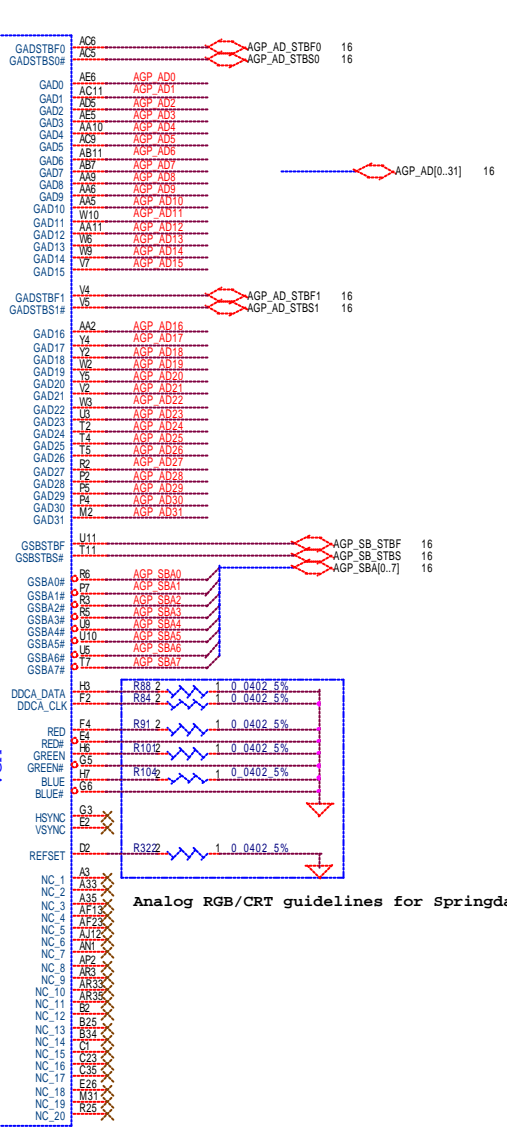
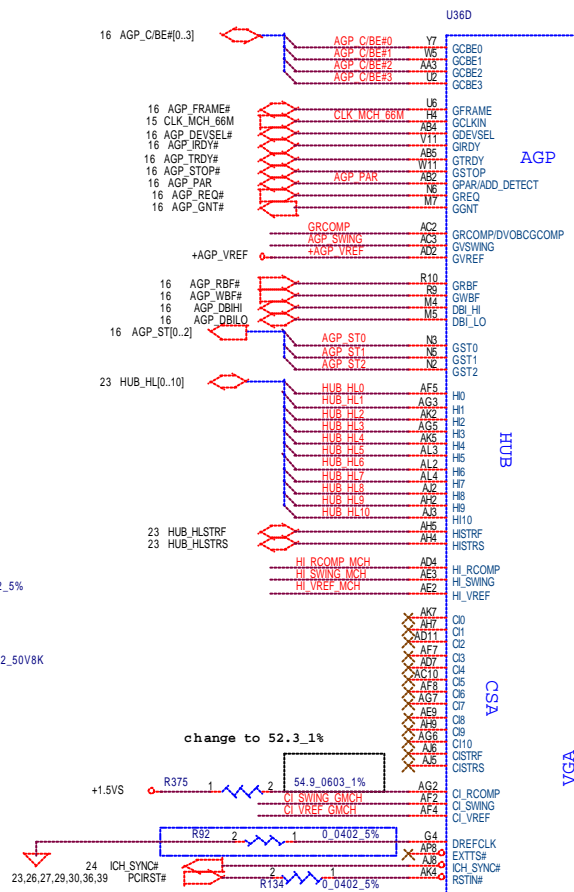
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1: External AGP
0: Internal Graphics



Note:
Springdale Customer Schematic R1.2 page18
AGP_SWING only had 0.1u cap ; But Springdale
Chipset Platform Design guide Rev1.11(12474)
page138 had a 0.01uf cap. need confirm with
Intel.

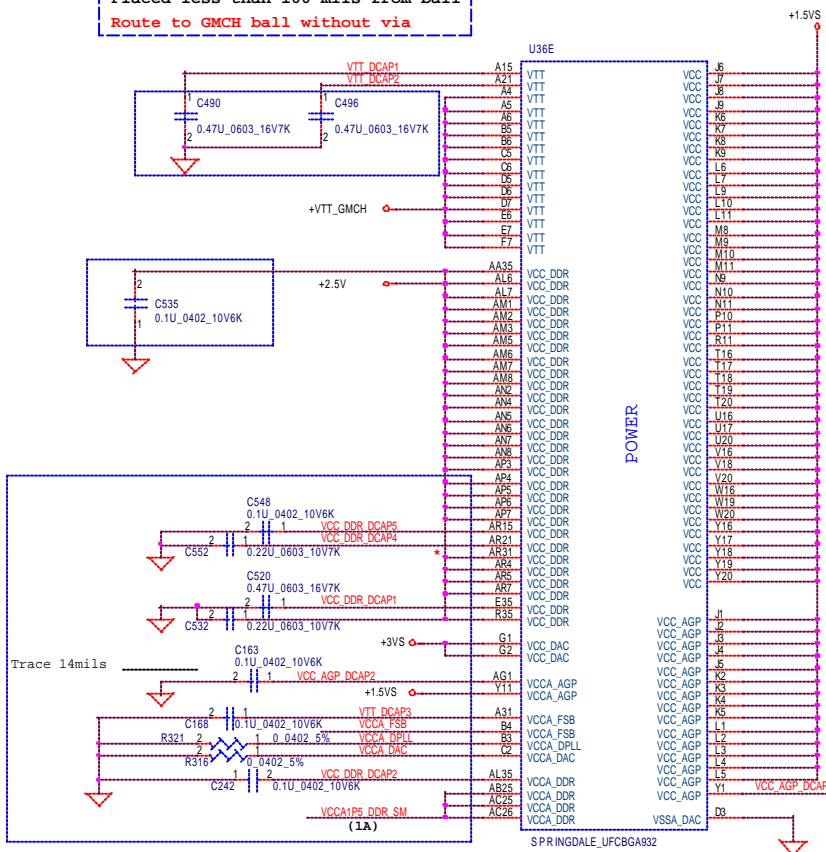


Analog RGB/CRT guidelines for Springdale-P

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Title Springdale-AGP/HUB/VGA/CSA (4/5)		
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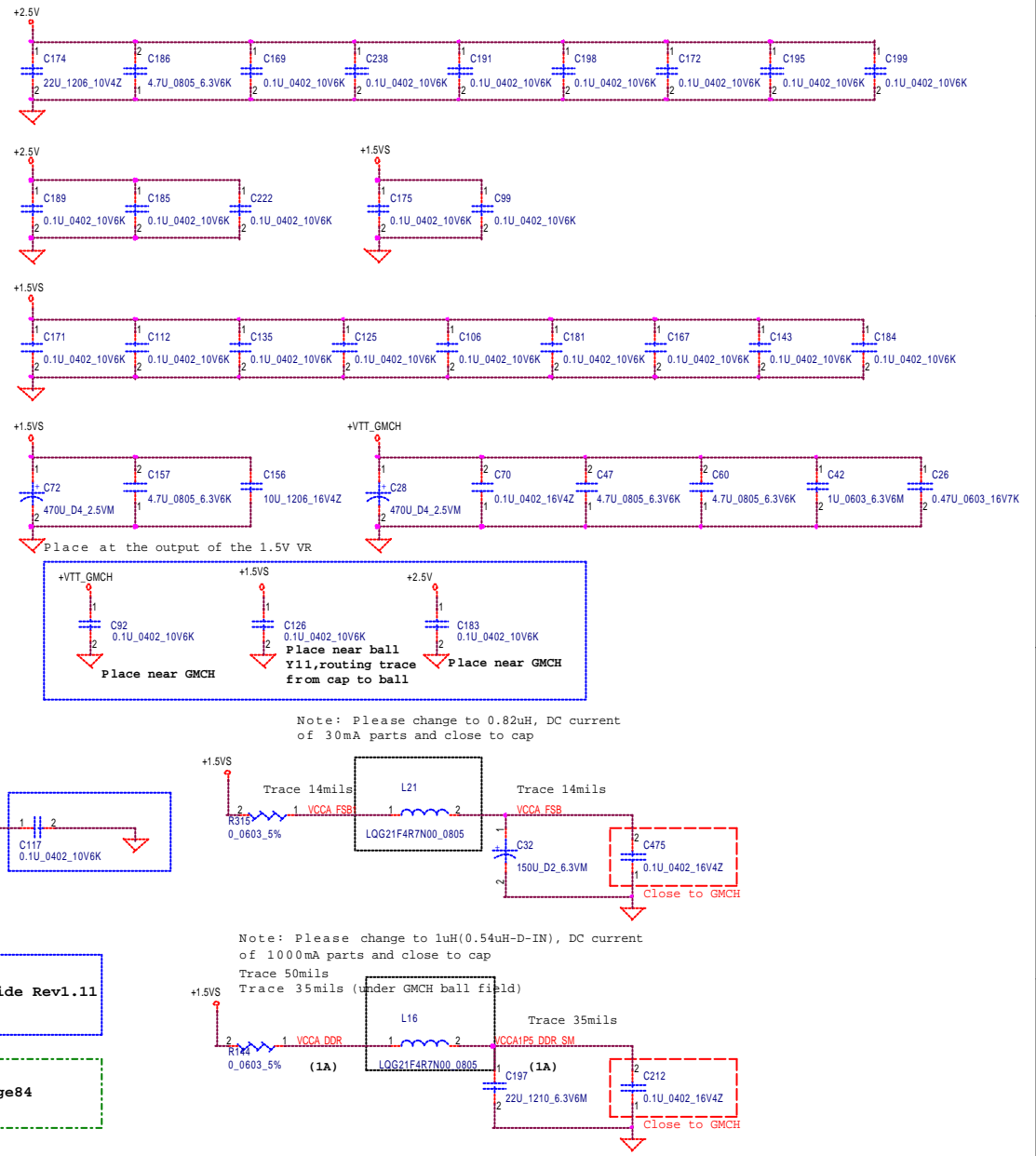
Note:
Placed less than 100 mils from ball
Route to GMCH ball without via



Note:
Placed less than 100 mils from ball
Route to GMCH ball without via

Decoupling Reference Document:
Springdale Chipset Platform Design guide Rev1.11
(12474)page246,248

Decoupling Reference Document:
Springdale Customer Schematic R1.2 page84

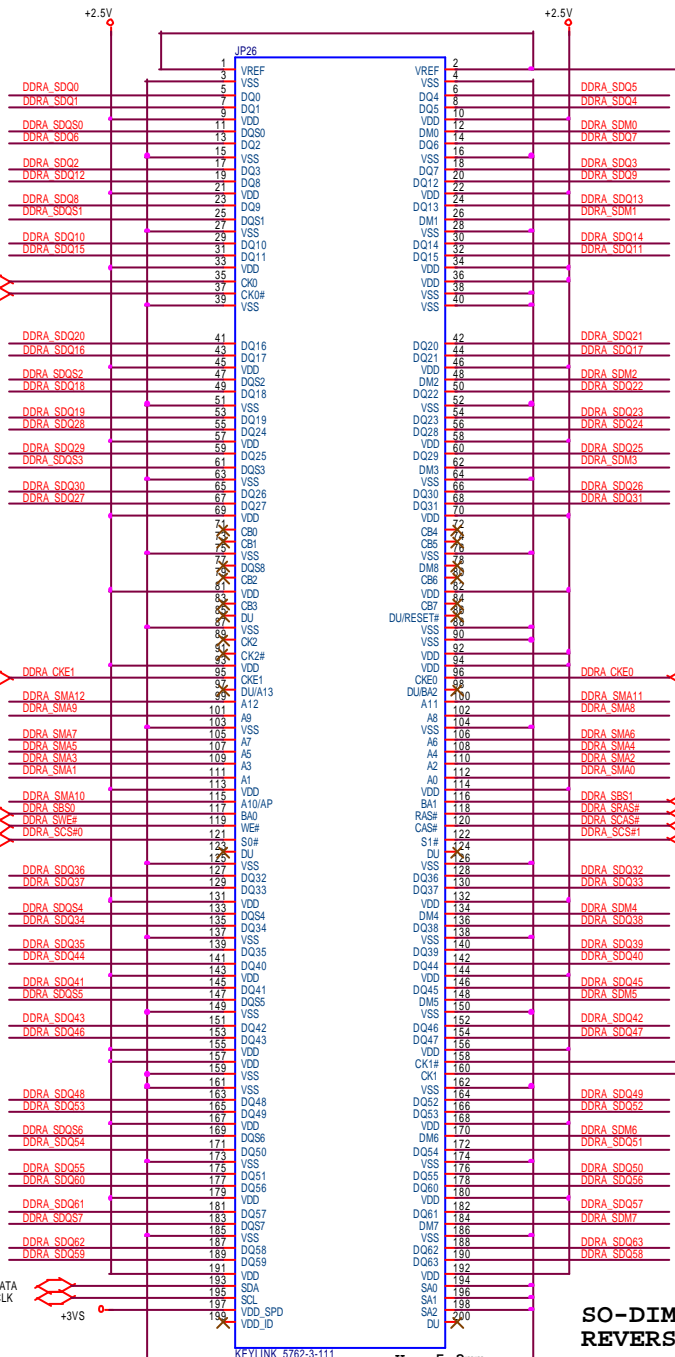


Note: Please change to 0.82uH, DC current of 30mA parts and close to cap

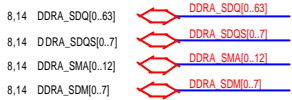
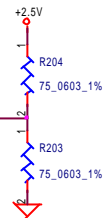
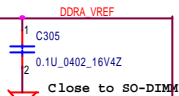
Note: Please change to 1uH(0.54uH-D-IN), DC current of 1000mA parts and close to cap

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Springdale-Decoupling (5/5)		
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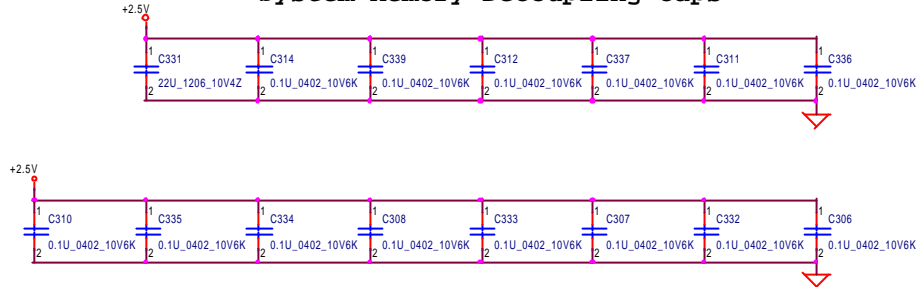
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DDRA_VREF trace width of 12mils and space 12mils(min)



System Memory Decoupling caps



Decoupling Reference Document:
Springdale Customer Schematic R1.2 page22
each Channel(two DIMMs) requirement 22uF*1 ; 0.1uF*14

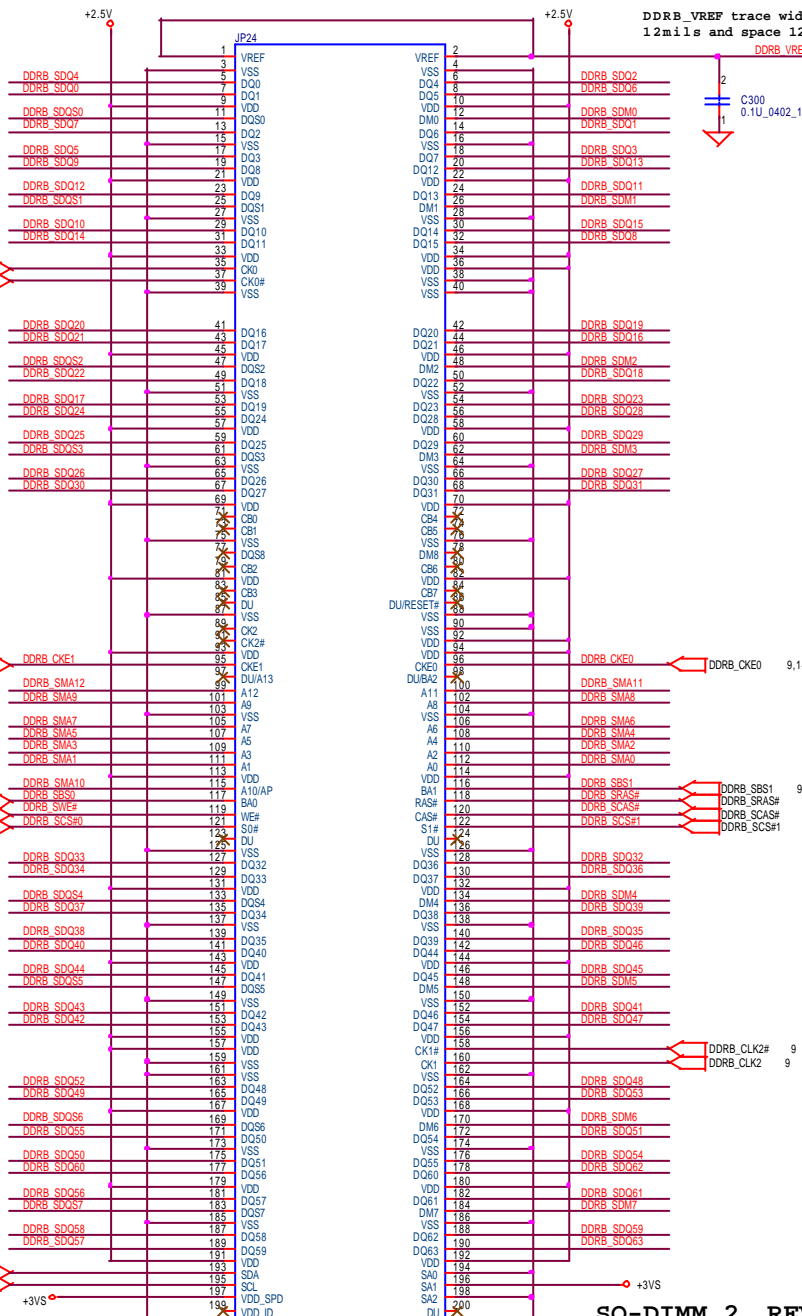
Decoupling Reference Document:
Springdale Chipset Platform Design guide Rev1.11
(12474)pag 271 each DIMM(two) requirement 0.1uF*42

SO-DIMM 0
REVERSE

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DDR-SODIMM SLOT1		
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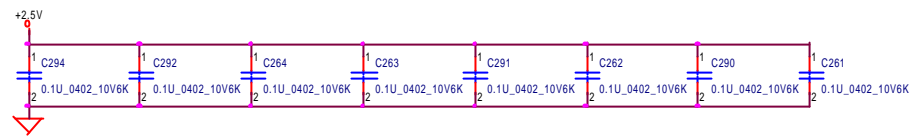
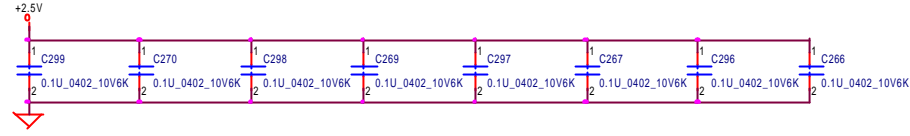
KEYLINK_5762-3-111 H = 5.2mm



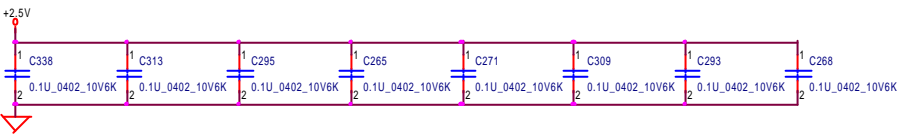
DDR_B_VREF trace width of 12mils and space 12mils(min)

- 9,14 DDRB_SDO[0..63] DDRB_SDO[0..63]
- 9,14 DDRB_SDO[0..7] DDRB_SDO[0..7]
- 9,14 DDRB_SMA[0..12] DDRB_SMA[0..12]
- 9,14 DDRB_SDM[0..7] DDRB_SDM[0..7]

System Memory Decoupling caps



Decoupling Reference Document:
Springdale Customer Schematic R1.2 page26
each Channel(two DIMMs) requirement 0.1uF*24



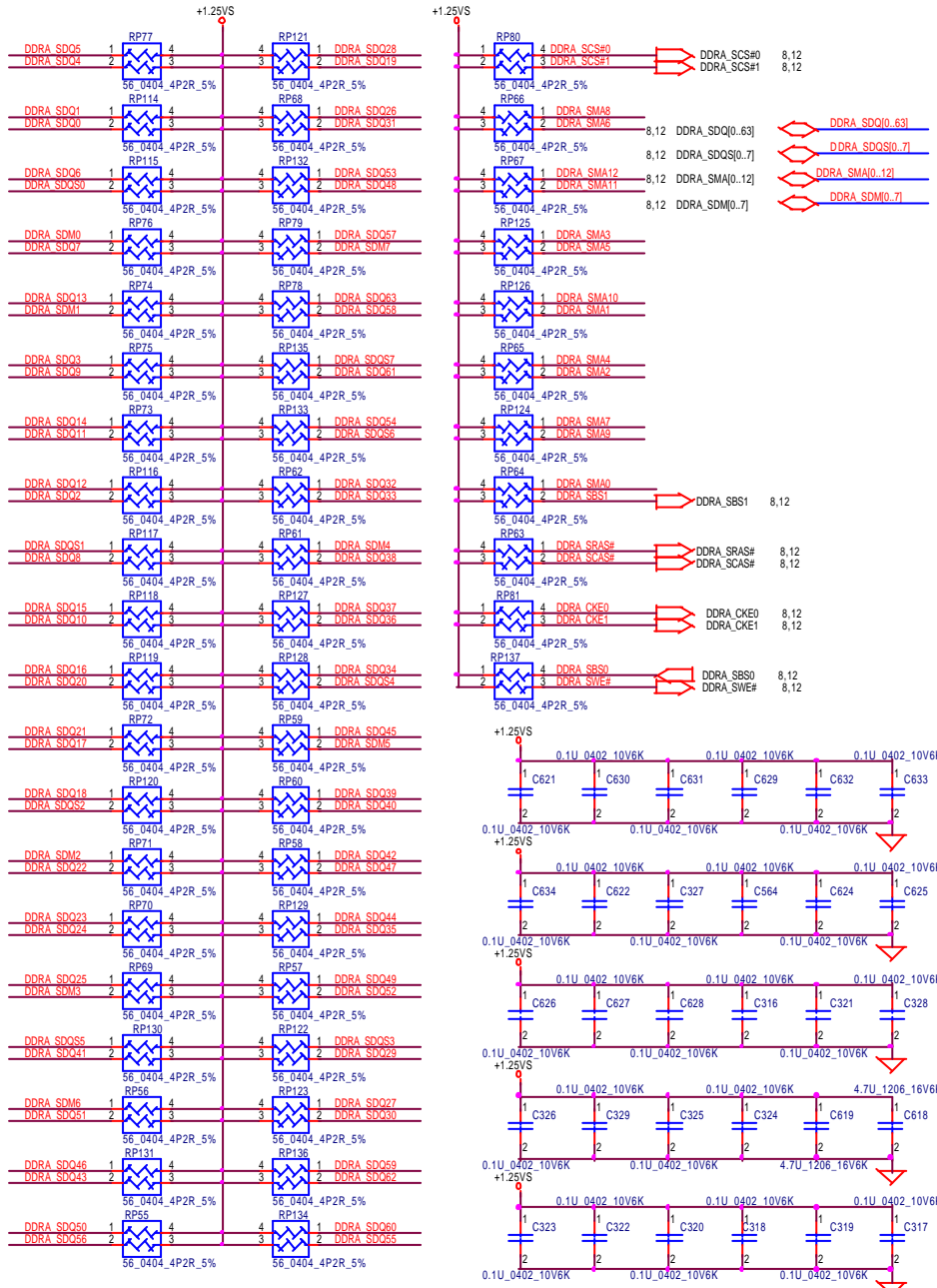
SO-DIMM 2 REVERSE

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DDR-SODIMM SLOT2		
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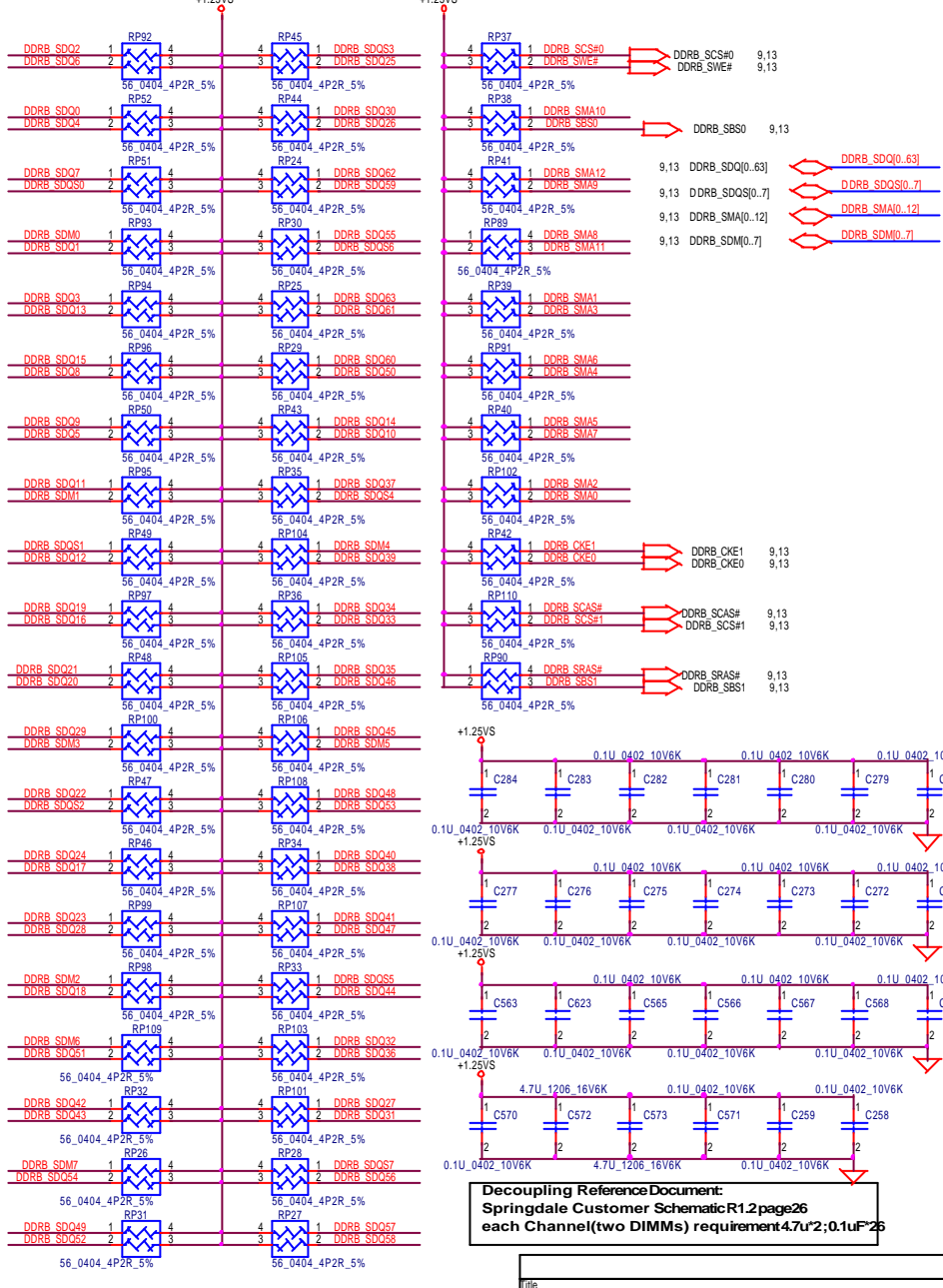
KLINK_5746-3-111
H = 9.2mm

Channel A(DIMM0) Termination resistors & Decoupling caps



Decoupling Reference Document:
Springdale Customer Schematic R1.2 page 22
each Channel (two DIMMs) requirement 4.7u*2; 0.1uF*28

Channel B (DIMM1) Termination resistors & Decoupling caps

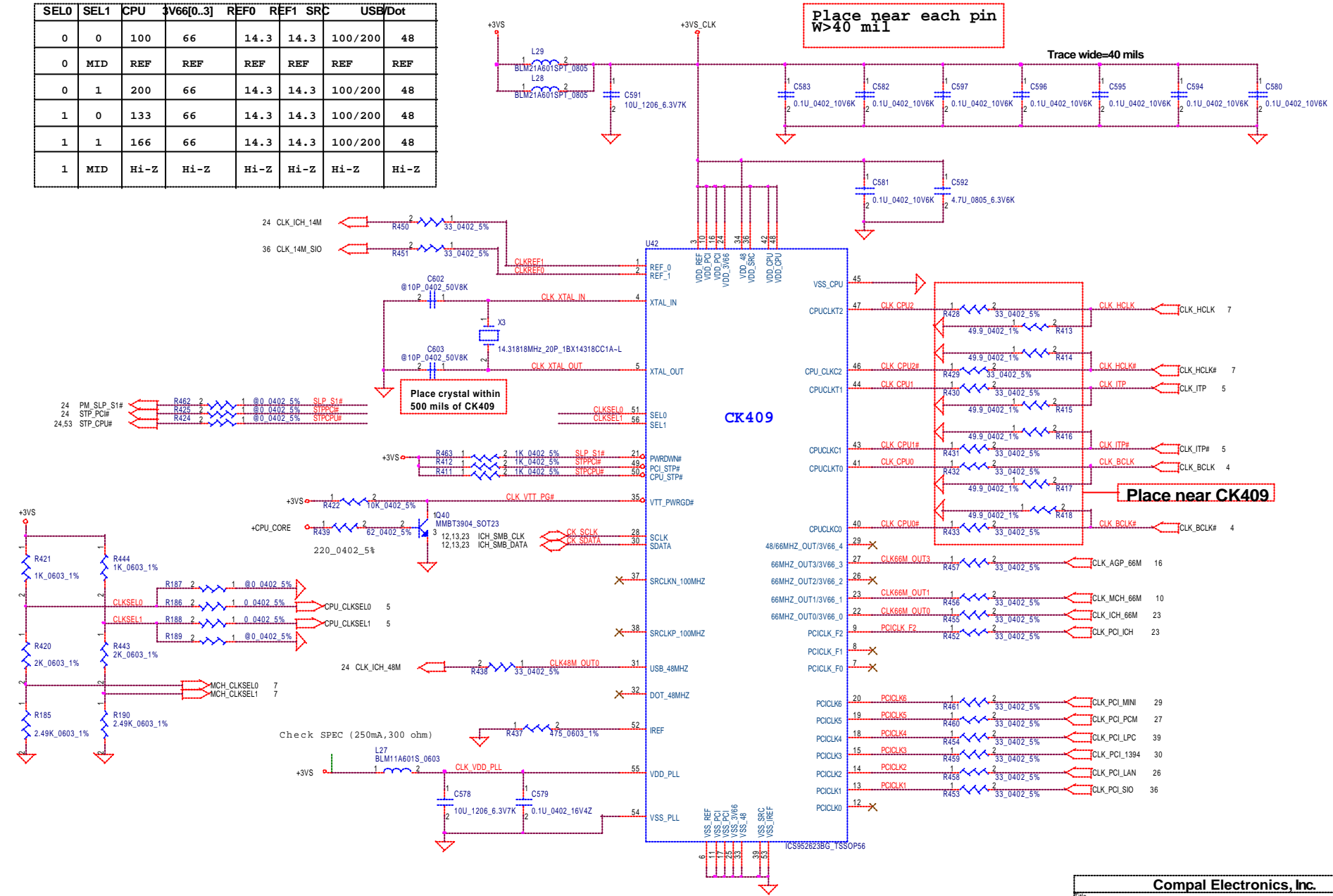


Decoupling Reference Document:
Springdale Customer Schematic R1.2 page 26
each Channel (two DIMMs) requirement 4.7u*2; 0.1uF*28

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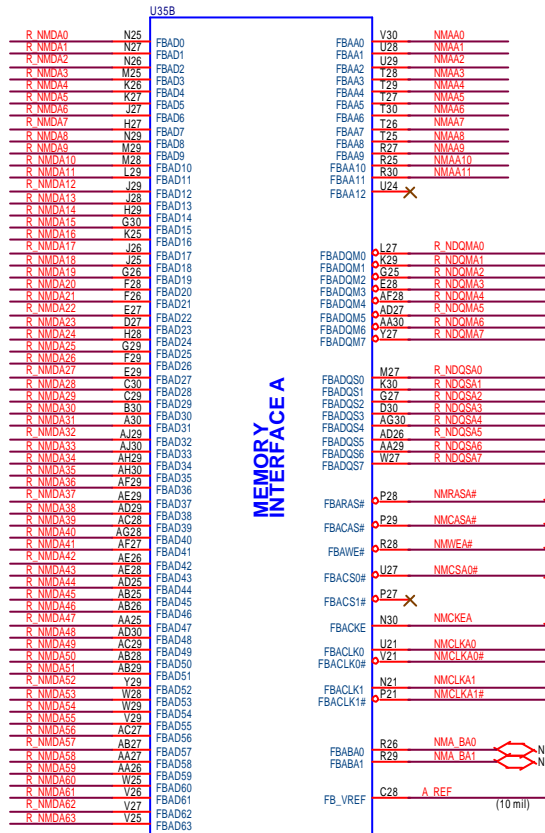
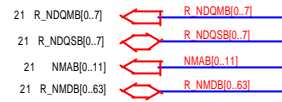
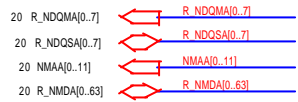
Title DDR Termination Resistors		
Size B	Document Number LA-1841	Rev 0.1
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SEL0	SEL1	CPU	V66[0..3]	REF0	REF1	SRC	USB/Dot
0	0	100	66	14.3	14.3	100/200	48
0	MID	REF	REF	REF	REF	REF	REF
0	1	200	66	14.3	14.3	100/200	48
1	0	133	66	14.3	14.3	100/200	48
1	1	166	66	14.3	14.3	100/200	48
1	MID	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

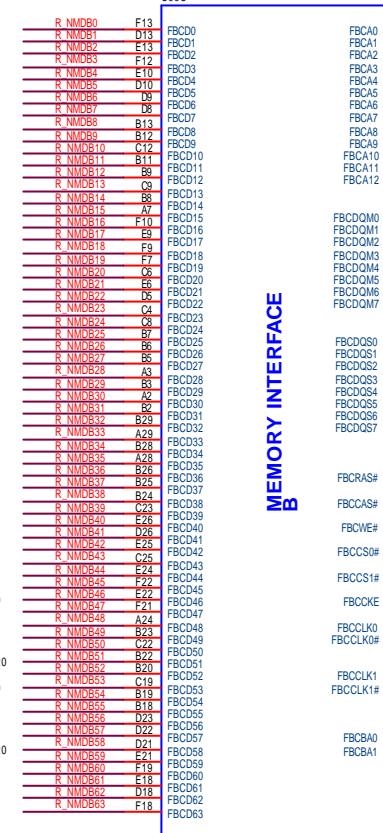


Compal Electronics, Inc.		
Clock Generator		
Title	Document Number	Rev
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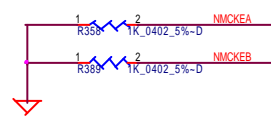
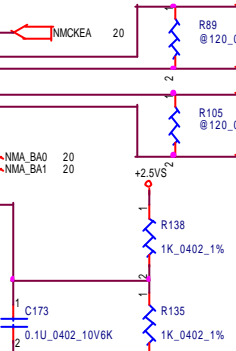
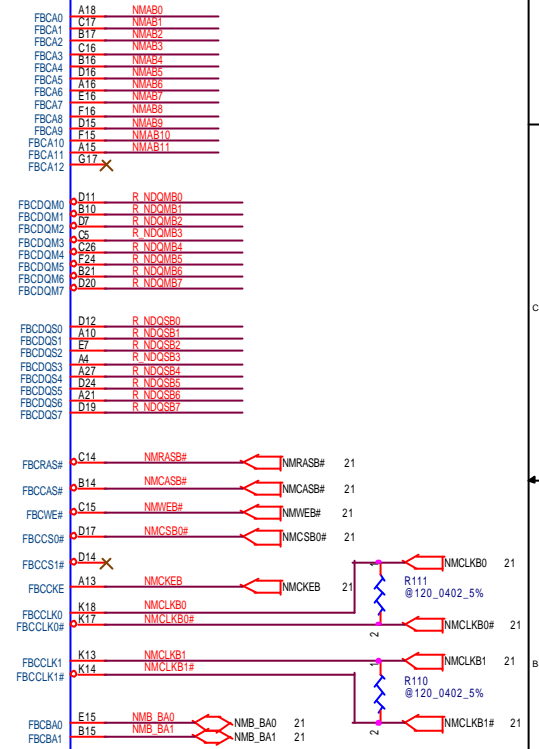
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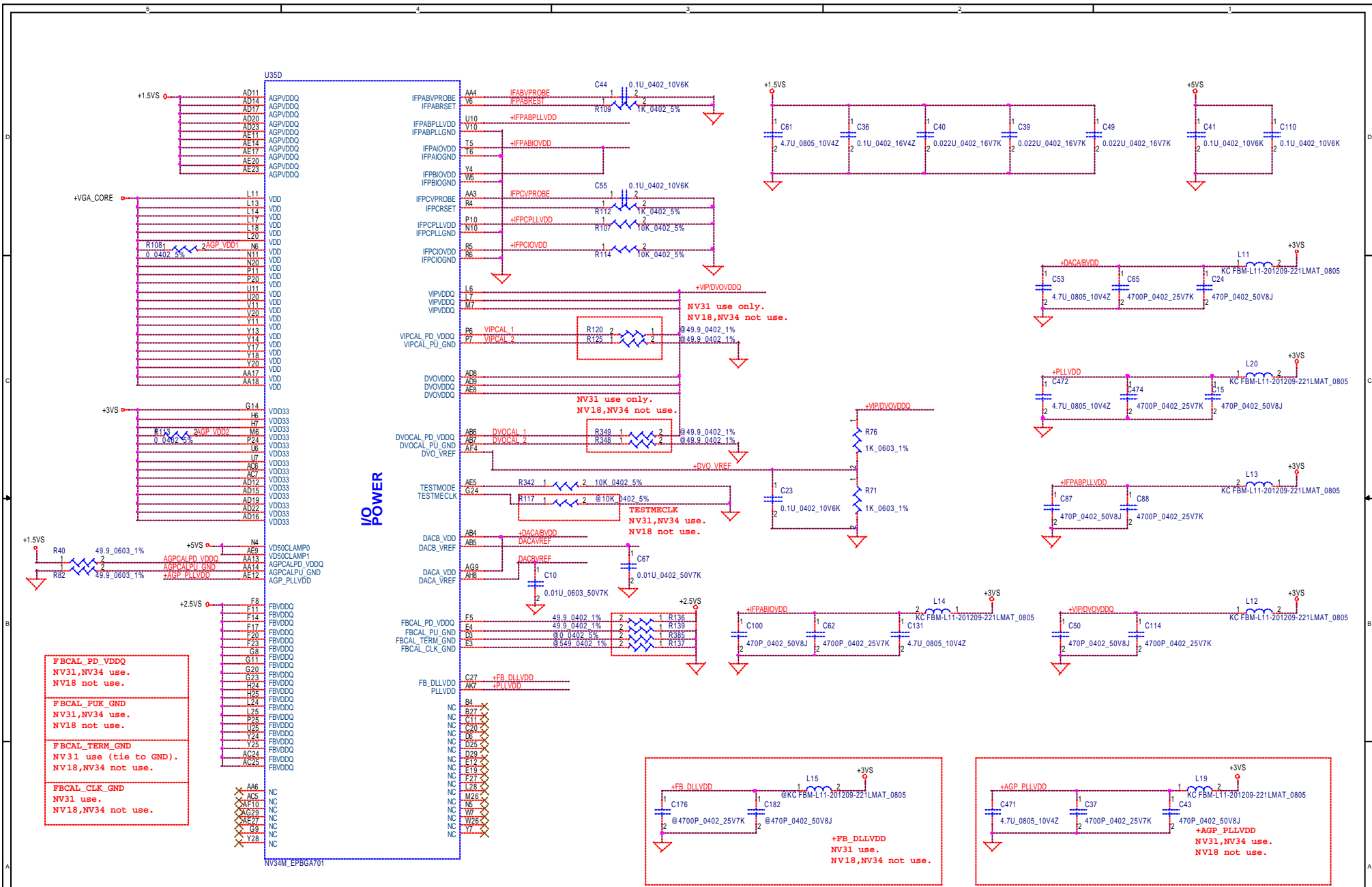


MEMORY INTERFACE A



MEMORY INTERFACE B





FB_CAL_PD_VDDQ
NV31, NV34 use.
NV18 not use.

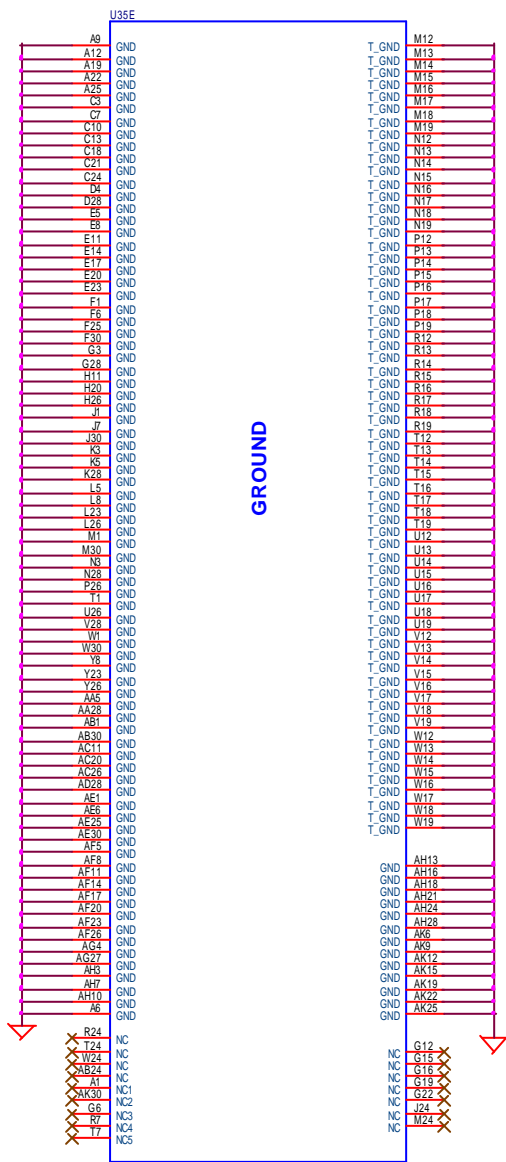
FB_CAL_PUK_GND
NV31, NV34 use.
NV18 not use.

FB_CAL_TERM_GND
NV31 use (tie to GND).
NV18, NV34 not use.

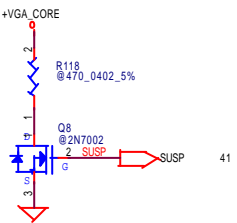
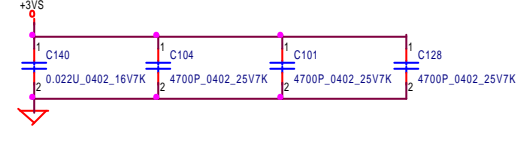
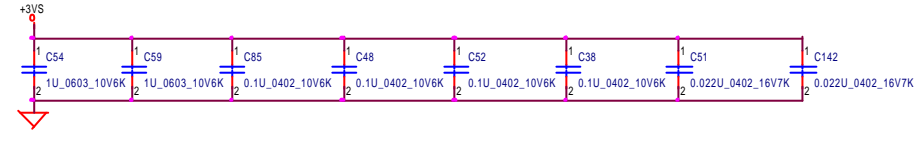
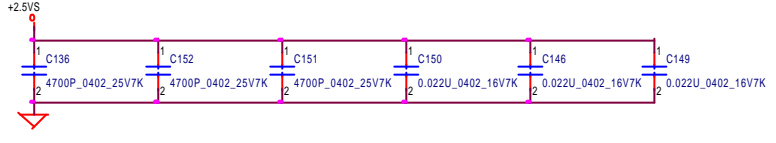
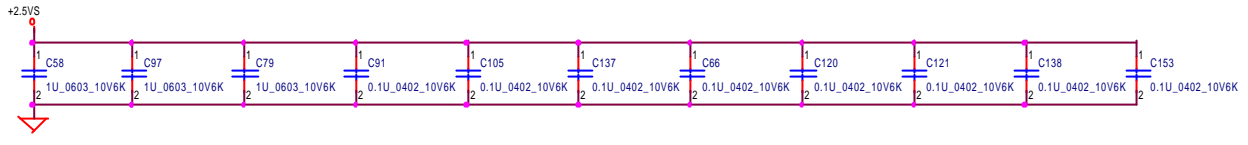
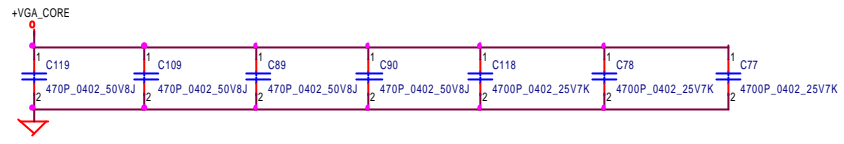
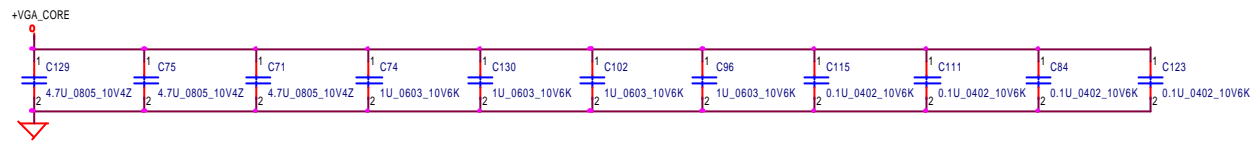
FB_CAL_CLK_GND
NV31 use.
NV18, NV34 not use.

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nVIDIA NV31M POWER			
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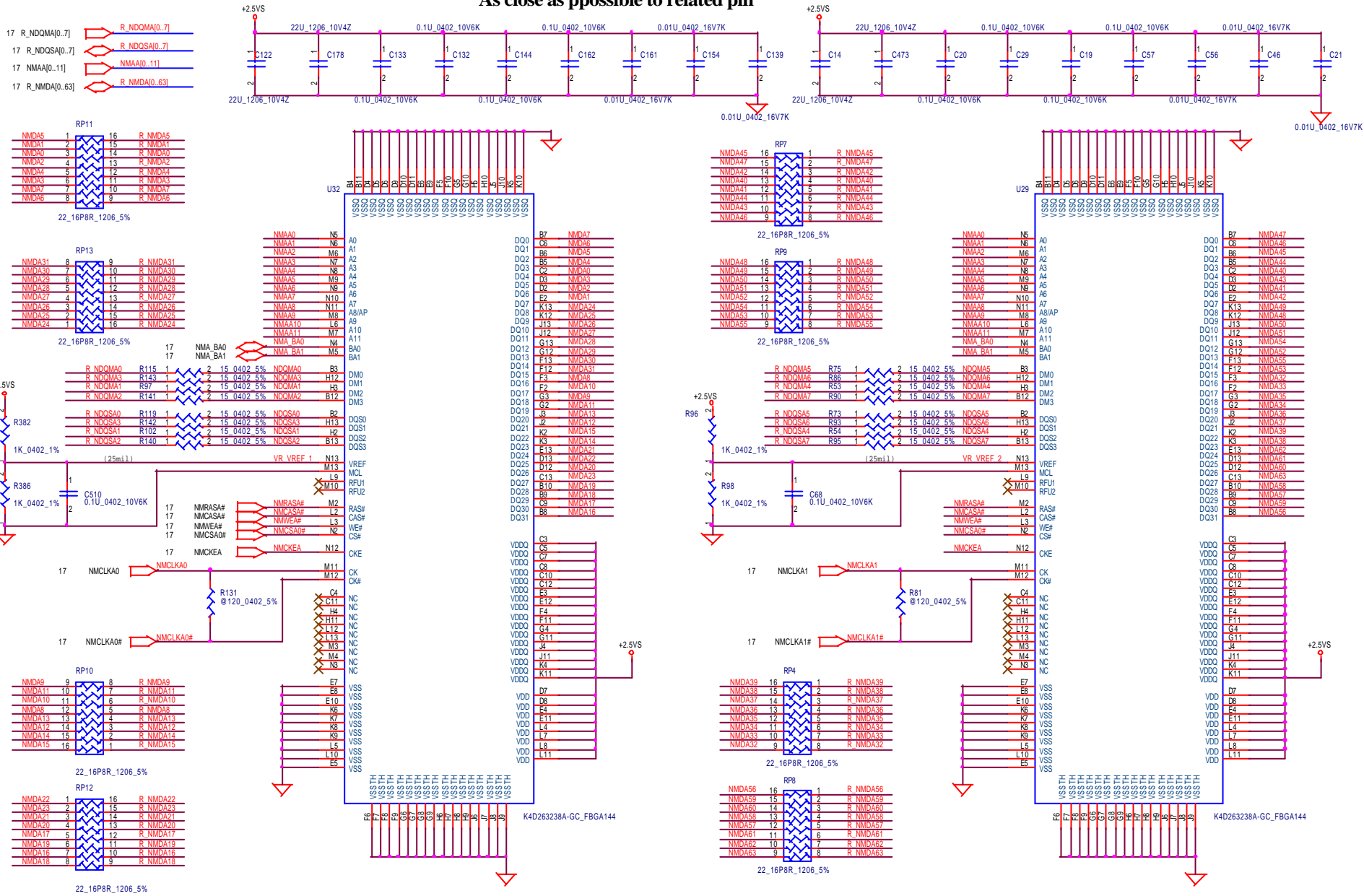
NV34M_EPBGA701



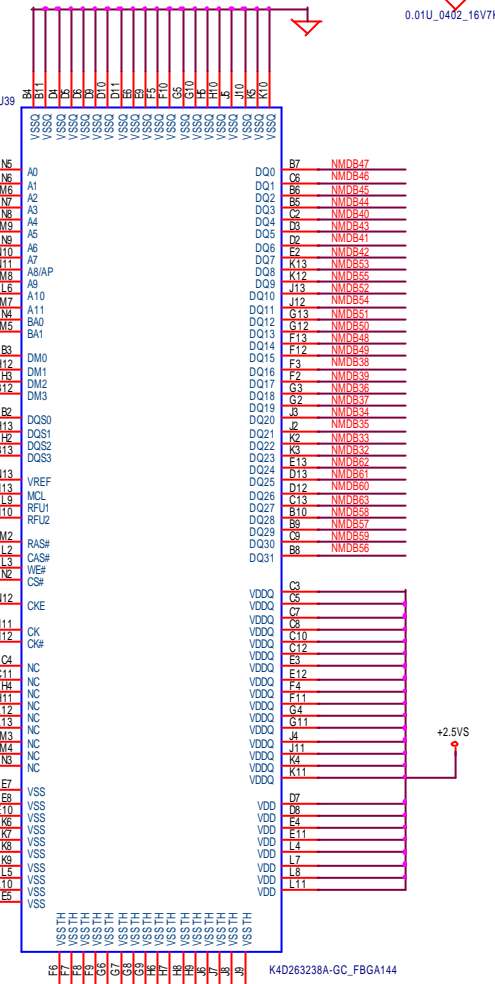
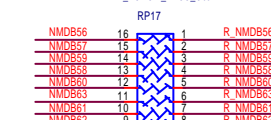
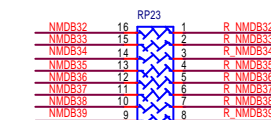
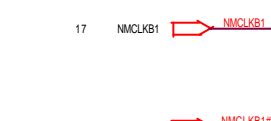
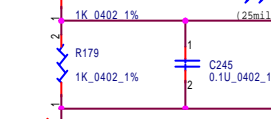
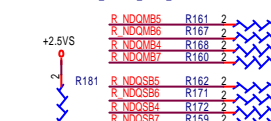
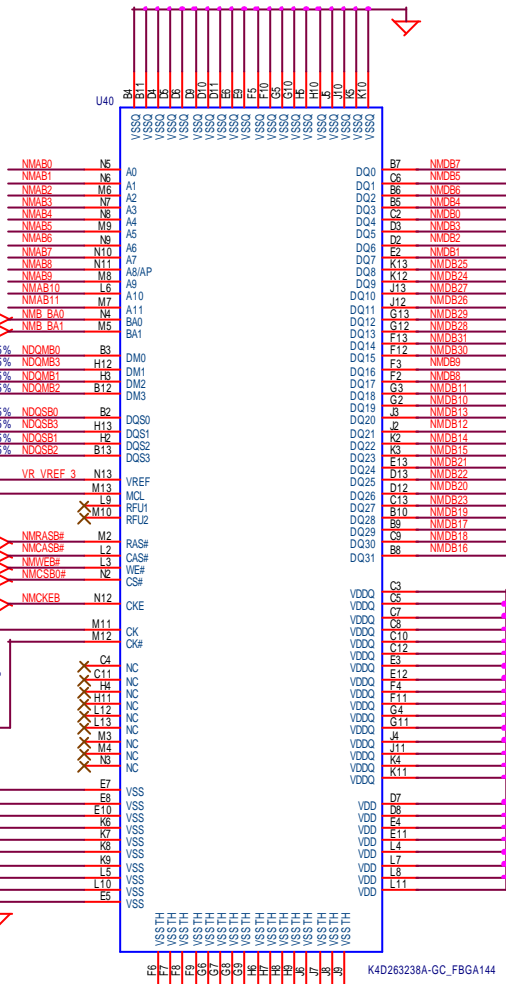
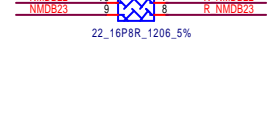
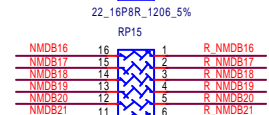
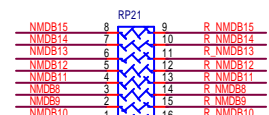
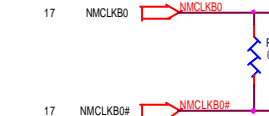
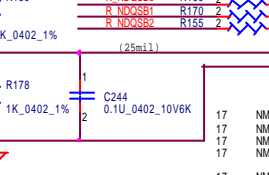
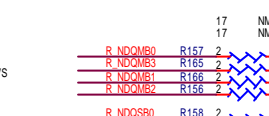
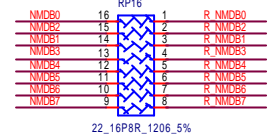
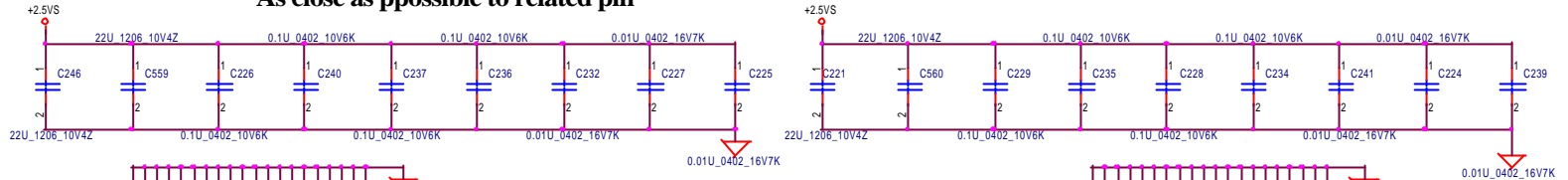
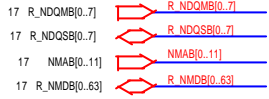
Compal Electronics, Inc.		
nVIDIA NV31M (DECOUPLING CAP)		
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As close as possible to related pin



As close as possible to related pin



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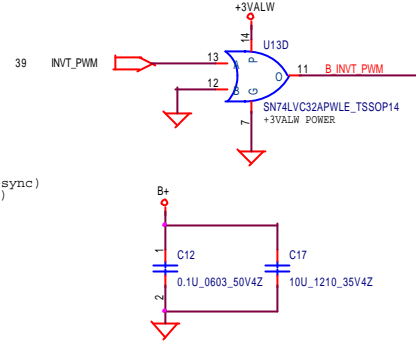
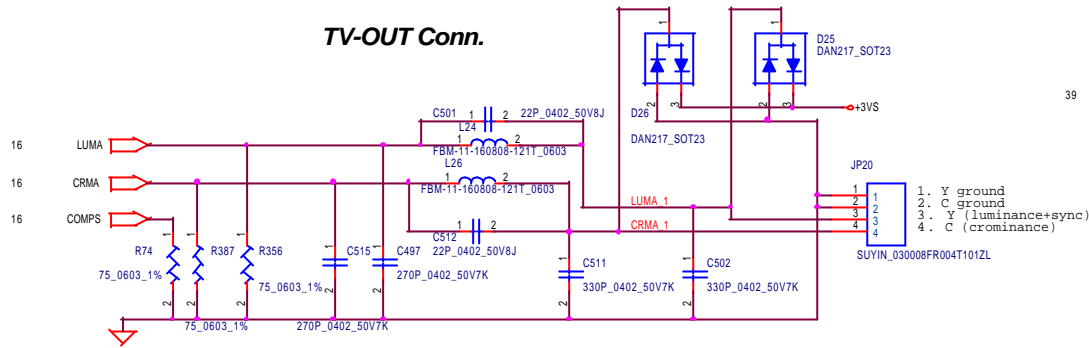
VGA DDR FOR CHANNEL B

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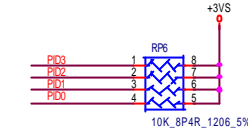
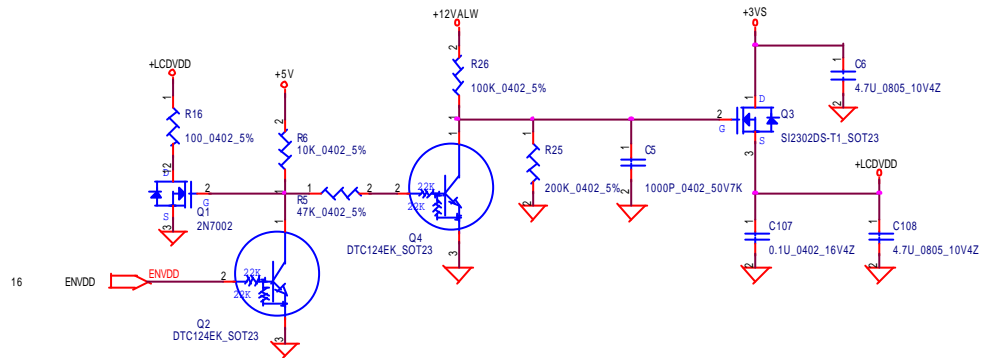
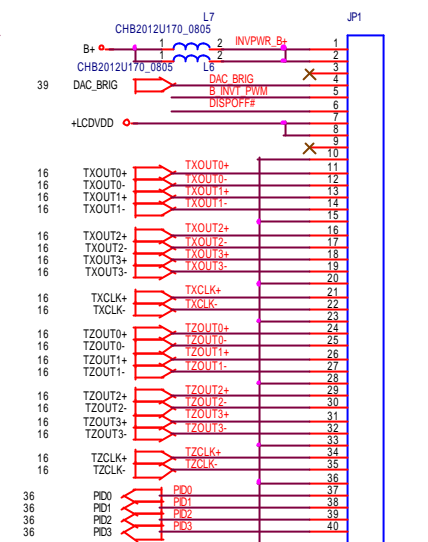
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CRT, TV-OUT & LVDS CONNECTOR

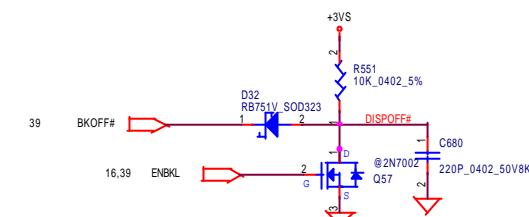
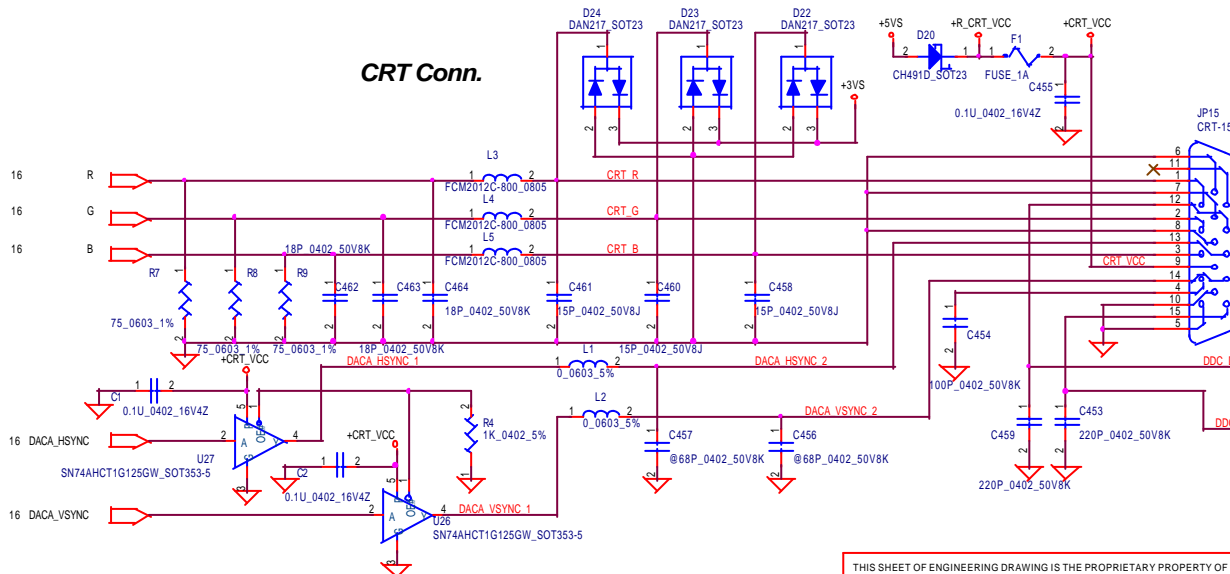
TV-OUT Conn.



LVDS Conn.

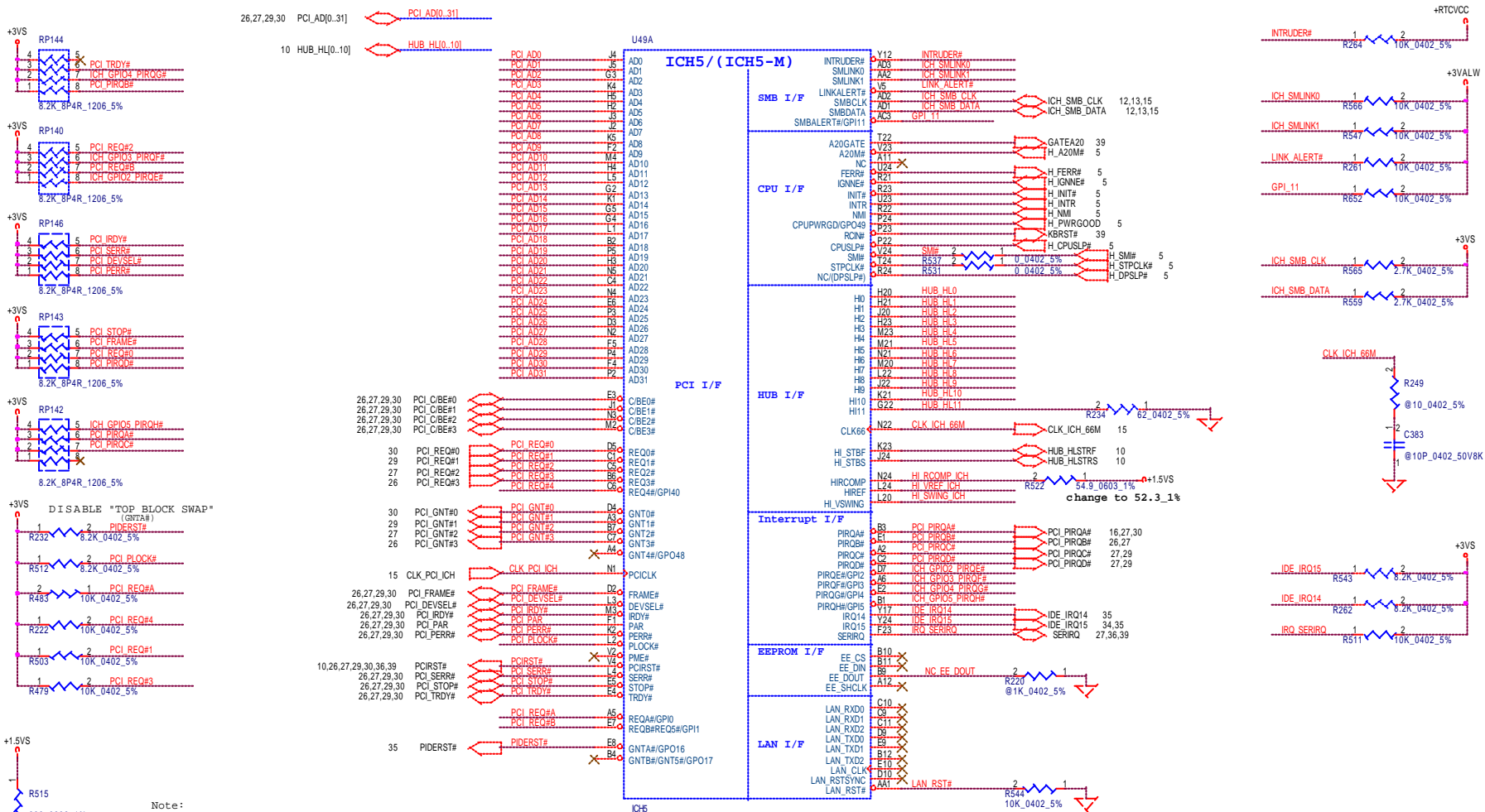


CRT Conn.

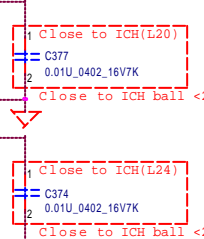


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Title CRT,TV-OUT & LVDS Connector		
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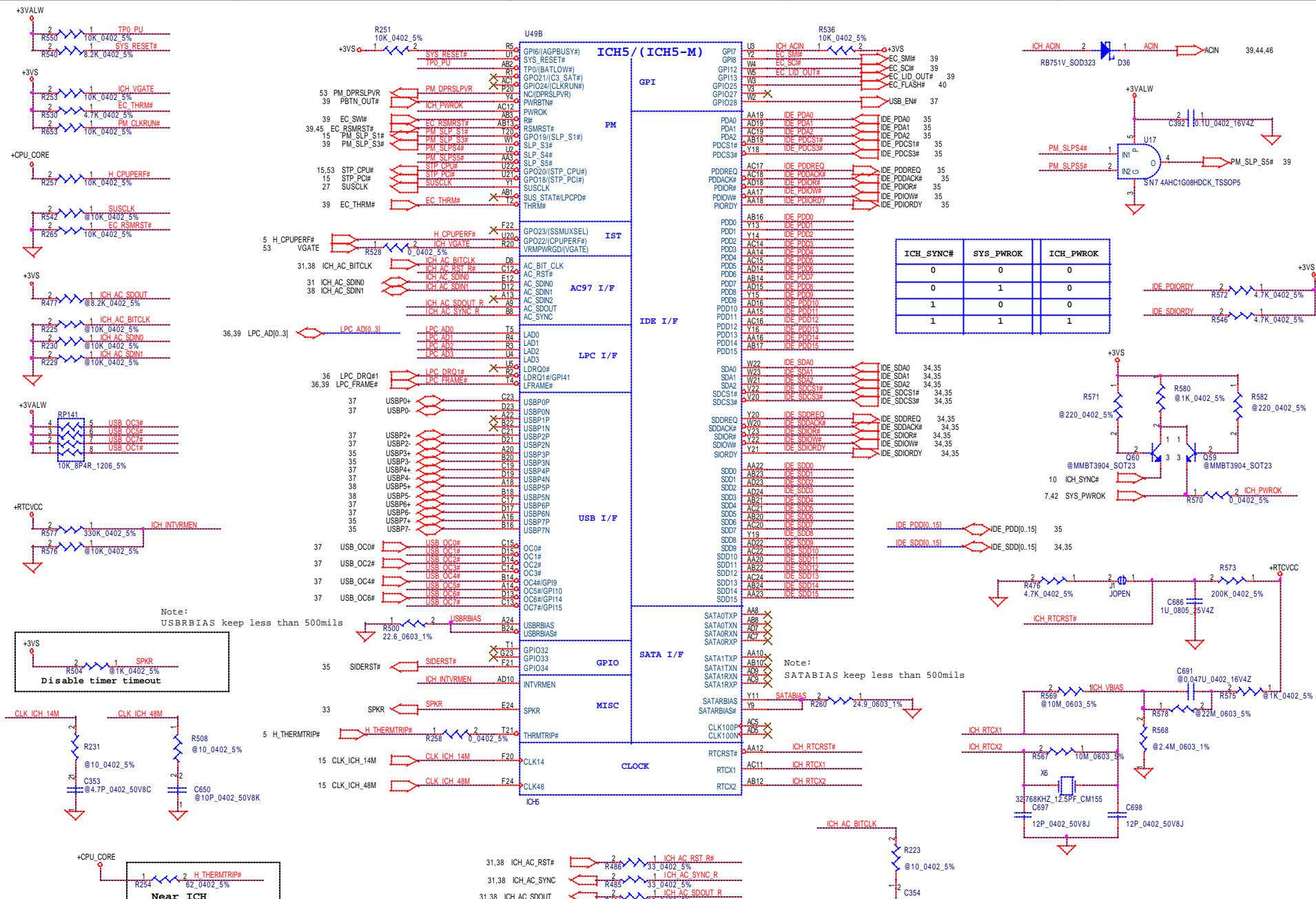


Note:
 HI_SWING_MCH, HI_VREF_MCH
 trace width of 10mils and
 space 7mils

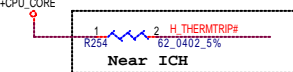
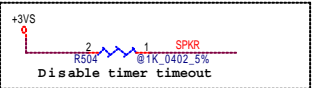
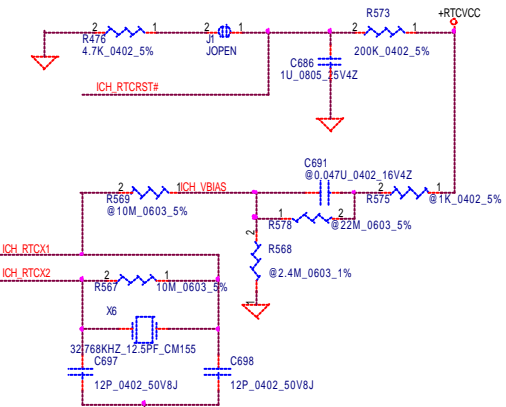
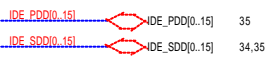
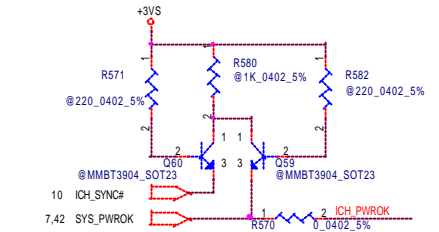
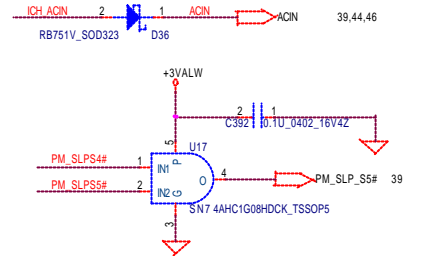


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Compal Electronics, Inc.			
ICH5-PCI/HUB/LAN			
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ICH_SYNC#	SYS_PWROK	ICH_PWROK
0	0	0
0	1	0
1	0	0
1	1	1



Note:
USBRBIAS keep less than 500mills

Note:
SATABIAS keep less than 500mills

26,27,29,30,36,39 PM_CLKRUN# <-> PM_CLKRUN#

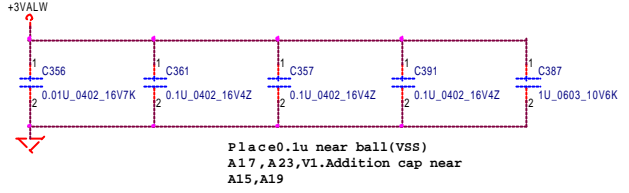
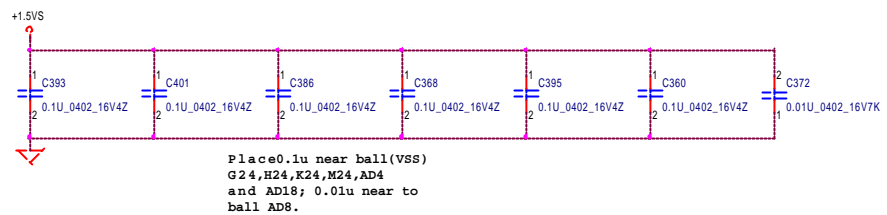
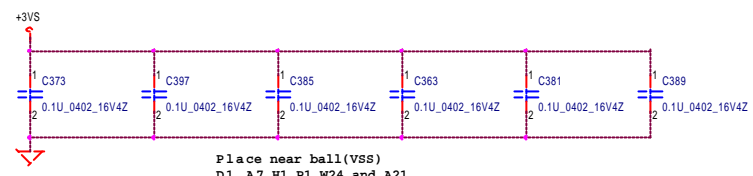
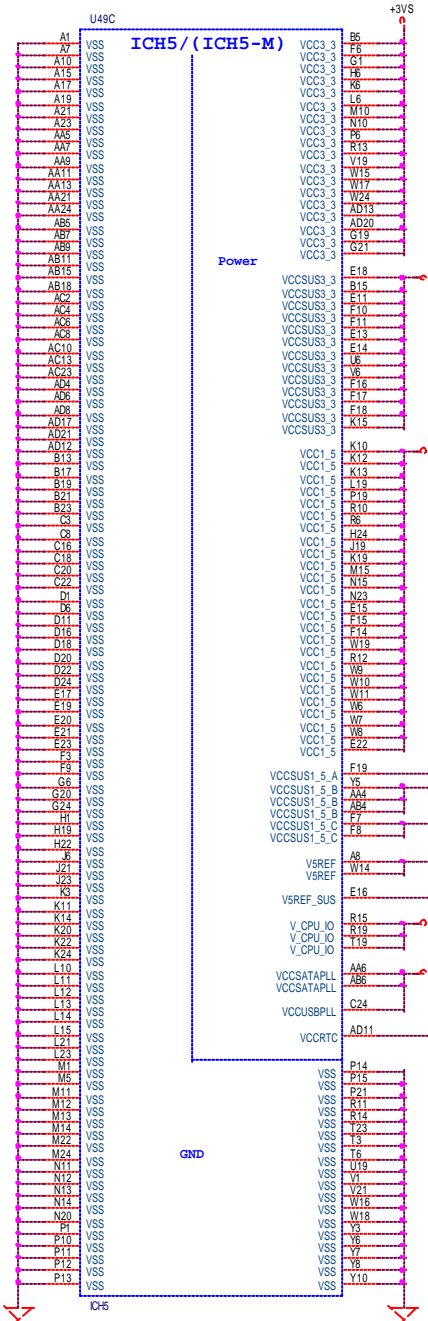
31,38 ICH_AC_RST# <-> ICH_AC_RST_R#
 31,38 ICH_AC_SYNC <-> ICH_AC_SYNC_R
 31,38 ICH_AC_SDOUT <-> ICH_AC_SDOUT_R

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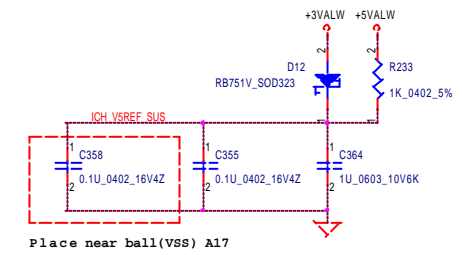
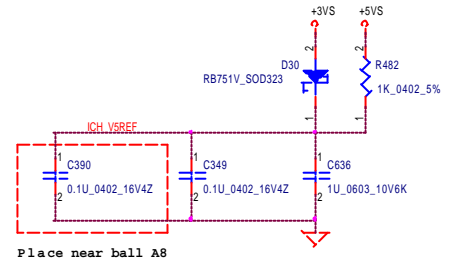
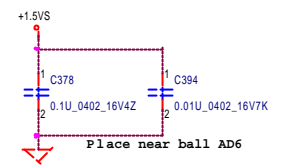
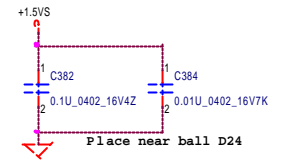
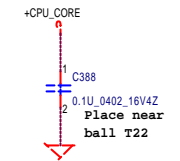
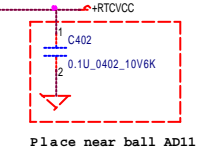
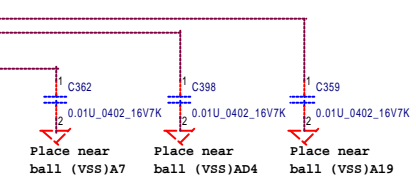
Compal Electronics, Inc.

ICH5-IDE/LPC/PM/GPIO/USB

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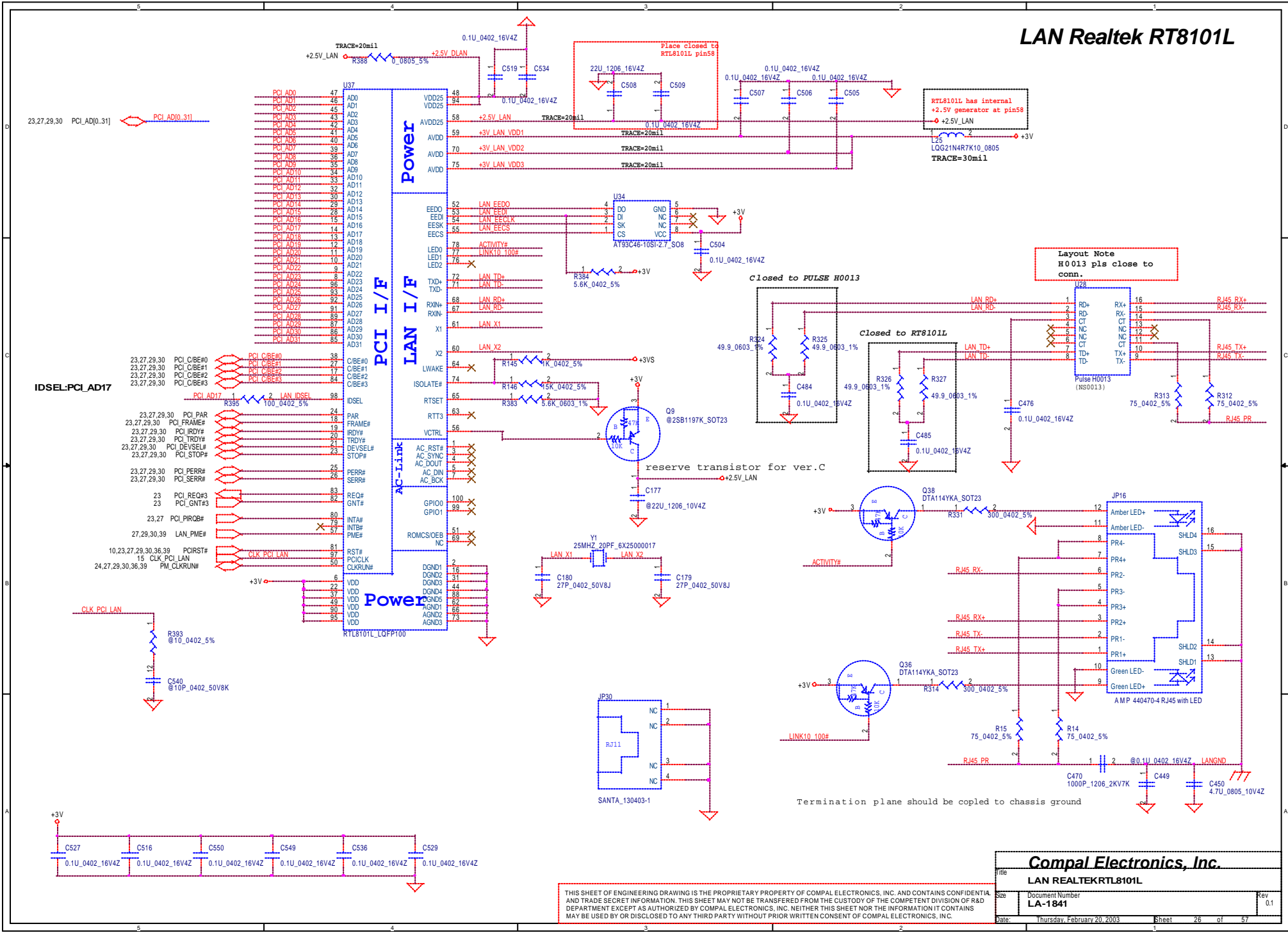
Decoupling Reference Document:
Springdale Chipset Platform Design guide Rev1.11
(12474)page278



Compal Electronics, Inc.		
ICH5 Power & Decoupling		
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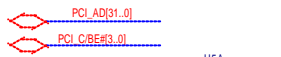
LAN Realtek RT8101L



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Compal Electronics, Inc.		
Title	LAN REALTEKRTL8101L	
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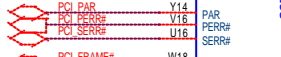
23,26,29,30 PCI_AD[31..0]
 23,26,29,30 PCI_CBE#[3..0]



- PCI_A0# K17
- PCI_A1# K18
- PCI_A2# K19
- PCI_A3# L17
- PCI_A4# L18
- PCI_A5# L19
- PCI_A6# L20
- PCI_A7# M17
- PCI_A8# M18
- PCI_A9# M19
- PCI_A10# M20
- PCI_A11# N17
- PCI_A12# N18
- PCI_A13# N19
- PCI_A14# N20
- PCI_A15# P17
- PCI_A16# P18
- PCI_A17# P19
- PCI_A18# P20
- PCI_A19# P16
- PCI_A20# R17
- PCI_A21# R18
- PCI_A22# R19
- PCI_A23# R20
- PCI_A24# T17
- PCI_A25# T18
- PCI_A26# T19
- PCI_A27# T20
- PCI_A28# U17
- PCI_A29# U18
- PCI_A30# U19
- PCI_A31# U20

- PCI_CBE#0 V20
- PCI_CBE#1 V19
- PCI_CBE#2 V18
- PCI_CBE#3 V17

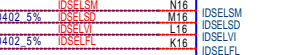
23,26,29,30 PCI_PAR
 23,26,29,30 PCI_PERR#
 23,26,29,30 PCI_SERR#



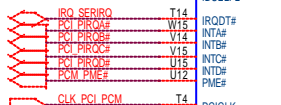
- PCI_FRAME# W18
- PCI_IRDY# W17
- PCI_TRDY# W18
- PCI_STOP# W16
- PCI_DEVSEL# W16
- PCI_REQ# W15
- PCI_GNT# W18
- PCI_CLKRUN# K20
- PCI_RST# K20

23,26,29,30 PCI_FRAME#
 23,26,29,30 PCI_IRDY#
 23,26,29,30 PCI_TRDY#
 23,26,29,30 PCI_STOP#
 23,26,29,30 PCI_DEVSEL#
 23 PCI_REQ#
 23 PCI_GNT#
 24,26,29,30,36,39 PCM_CLKRUN#
 10,23,26,29,30,36,39 PCIRST#

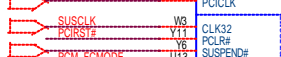
PCI_AD22 R402
 PCI_AD20 R403
 PCI_AD21 R407



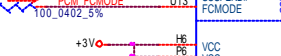
23,36,39 SERIRQ
 16,23,30 PCI_PIRQA#
 23,26 PCI_PIRQB#
 23,29 PCI_PIRQC#
 23,29 PCI_PIROD#
 26,29,30,39 PCM_PME#



15 CLK_PCI_PCM
 24 SUSCLK
 39 PCM_SUSP#



CLK_PCI_PCM R445
 33_0402_5%

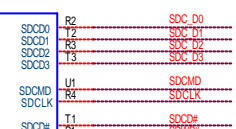


- H6 VCC
- P15 VCC
- R5 VCC
- R6 VCC
- R7 VCC
- R15 VCC
- R16 VCC
- T6 VCC
- T15 VCC

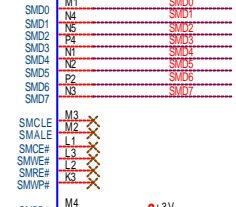
- L9 GND
- L10 GND
- L11 GND
- L12 GND
- M9 GND
- M10 GND
- M11 GND
- M12 GND

Power Supply
 TC6385XB_PBG328

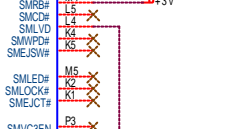
SP Interface



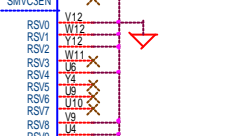
SmartMedia Interface



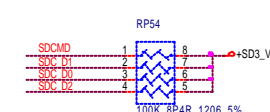
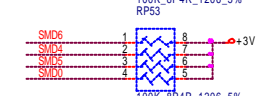
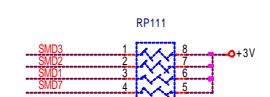
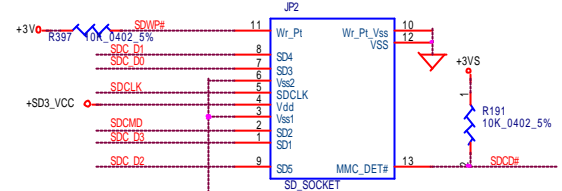
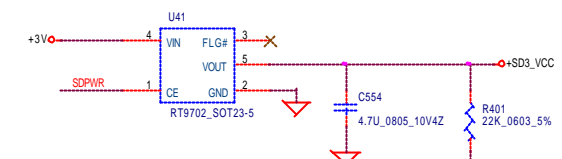
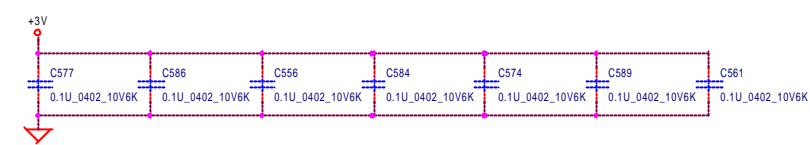
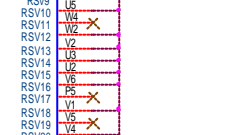
PCI Interface



Other pins

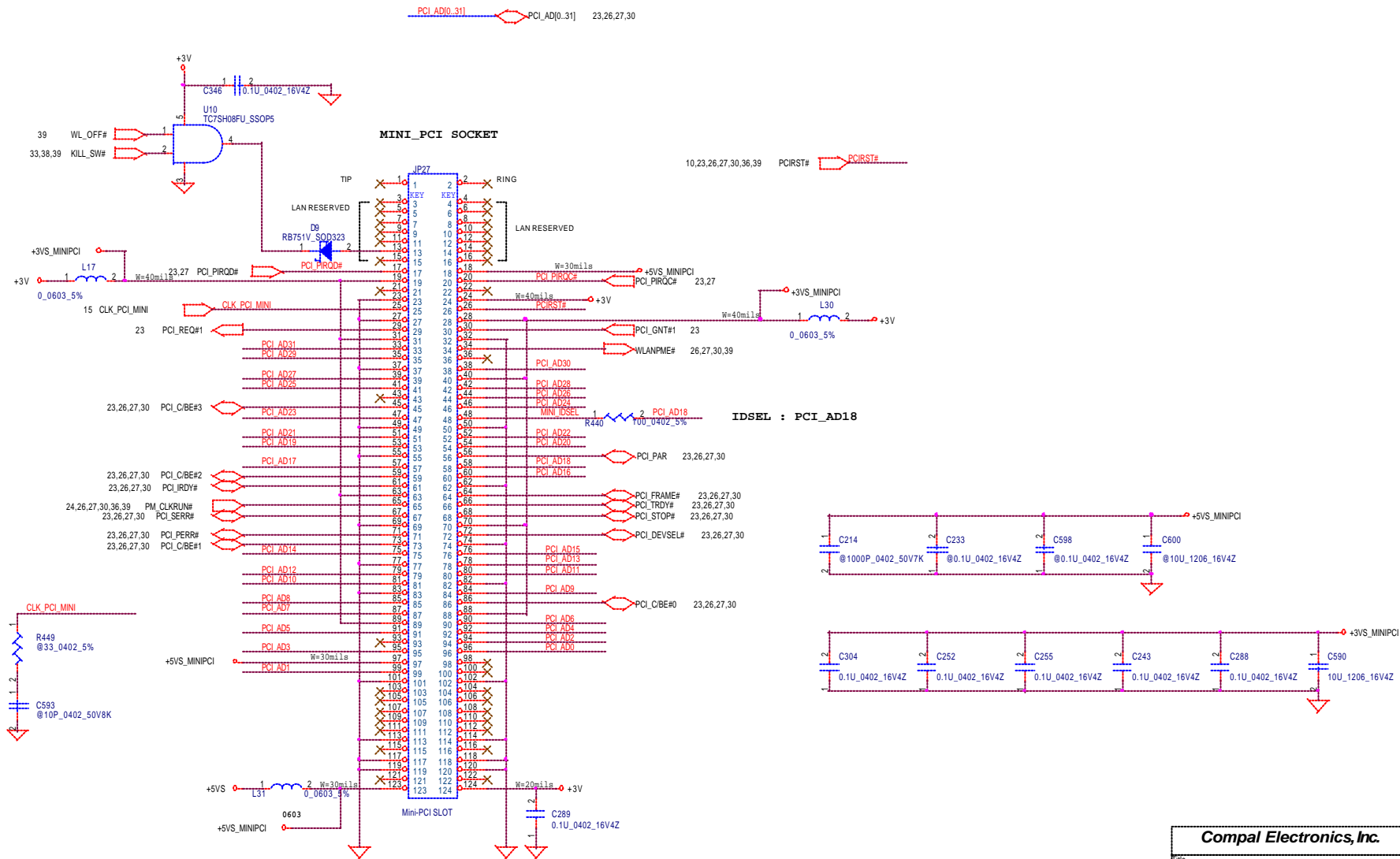


GPIO Interface



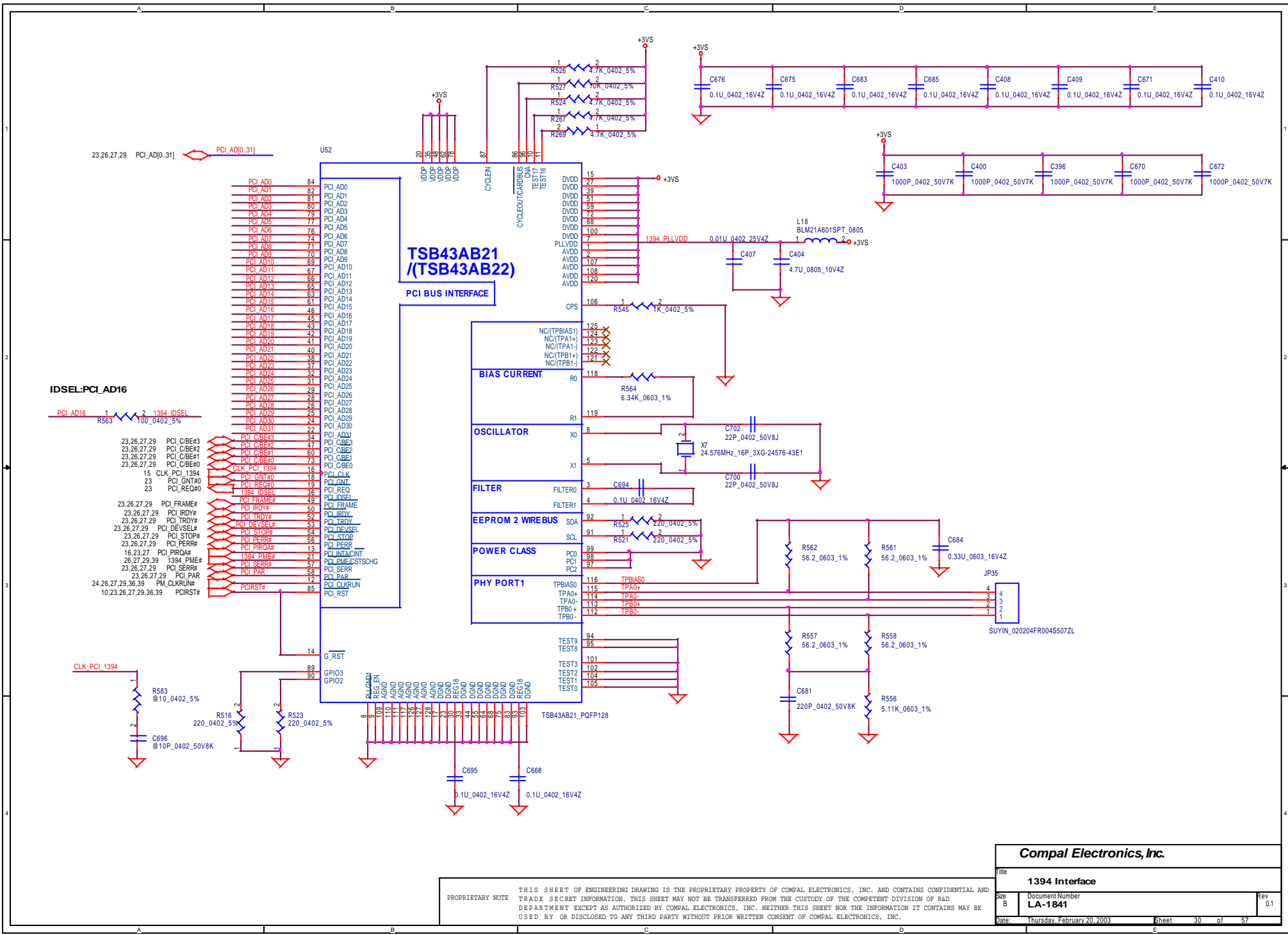
Compal Electronics, Inc.		
Title: CARDBUS & SD CONN (1/2)		
Size: B	Document Number: LA-1841	Rev: 0.1
Date: Thursday, February 20, 2003	Sheet: 27	of: 57

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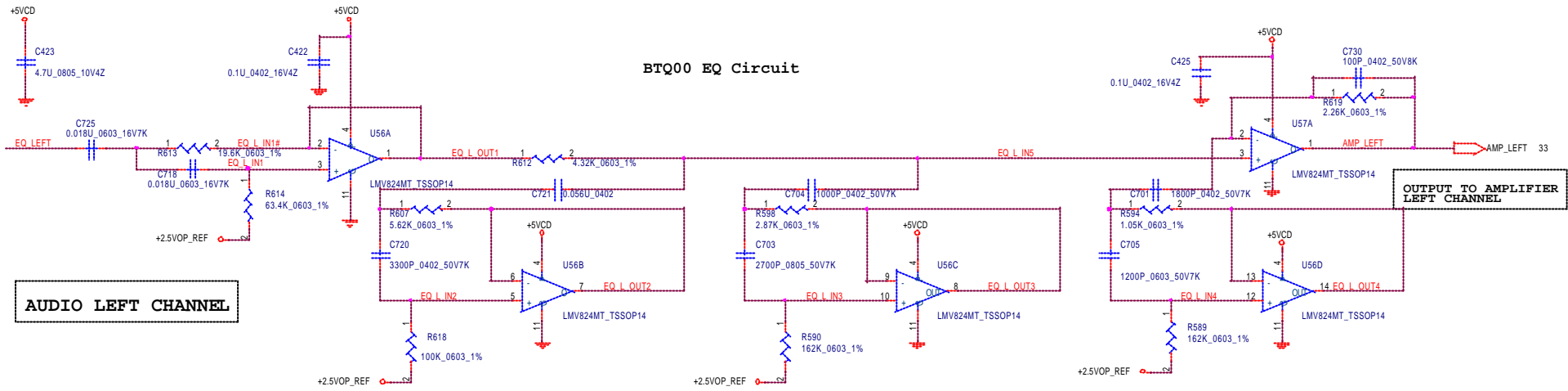
Compal Electronics, Inc.			
Title			
MINI_PCI			
Size	Document Number	Rev	
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Compal Electronics, Inc.			
Title: 1394 Interface			
Size: B	Document Number: LA-1841	Rev: 0.1	
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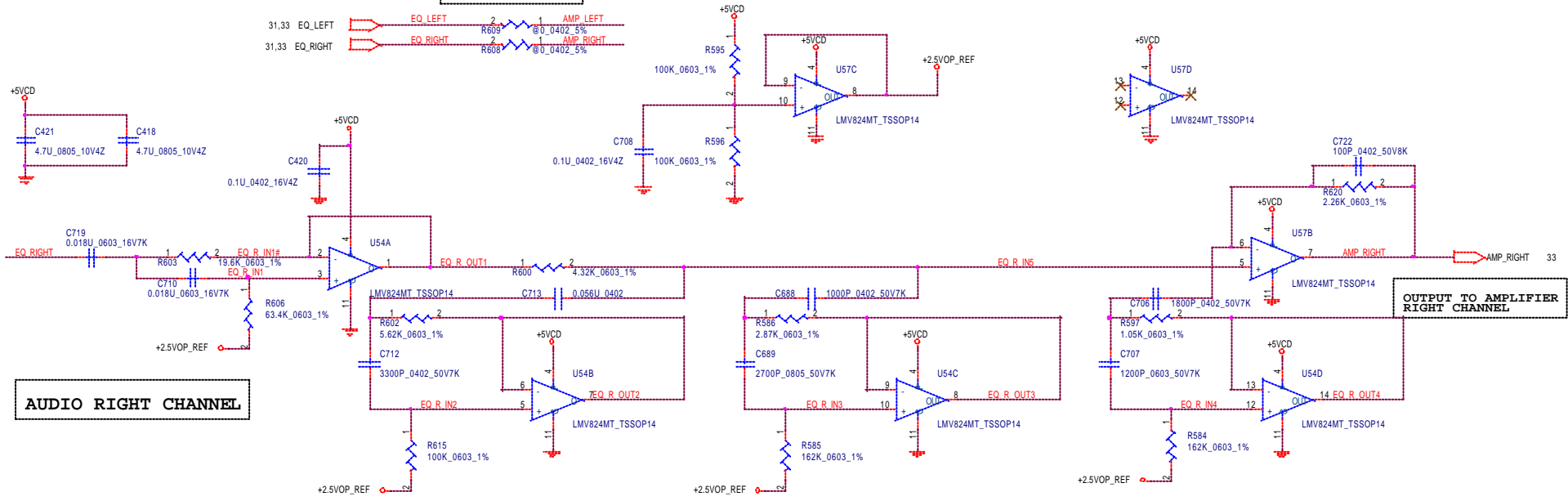
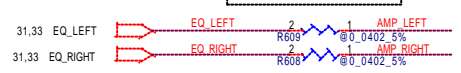
BTQ00 EQ Circuit



AUDIO LEFT CHANNEL

OUTPUT TO AMPLIFIER LEFT CHANNEL

BY-PASS EQ CIRCUIT



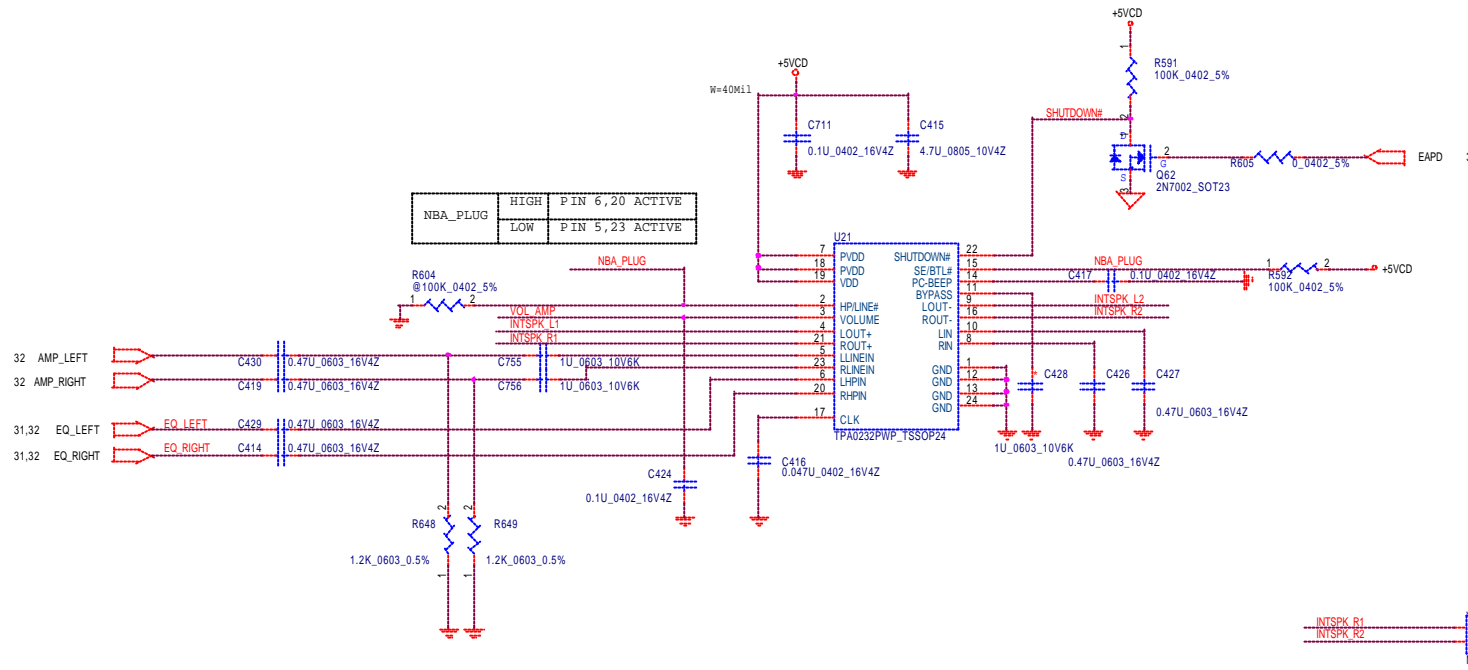
AUDIO RIGHT CHANNEL

OUTPUT TO AMPLIFIER RIGHT CHANNEL

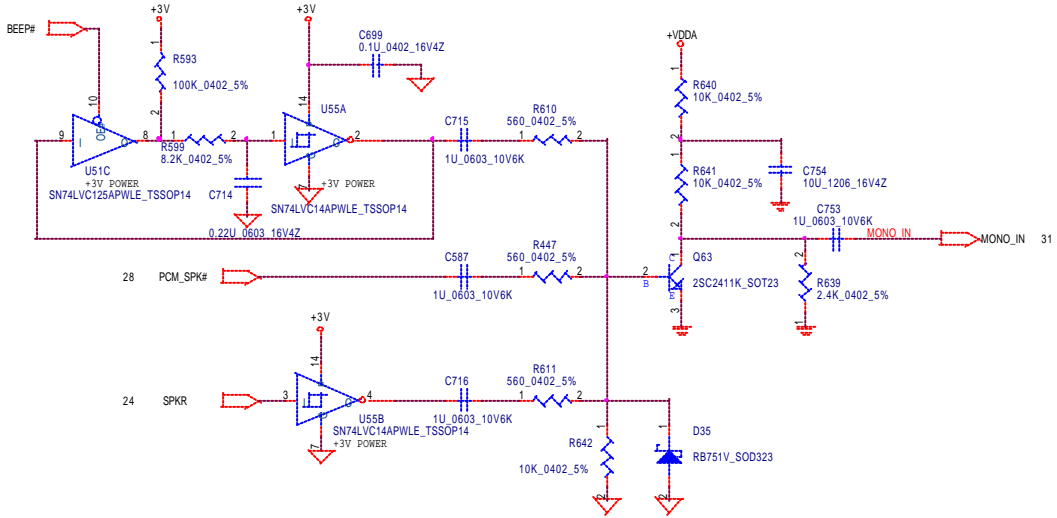
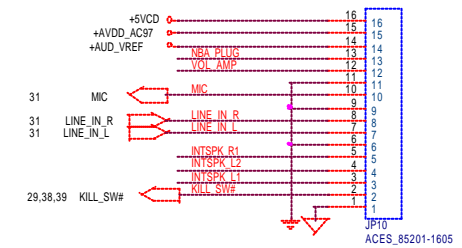
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Compal Electronics, Inc.		
Title HAREWAREEQ		
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Audio AMP

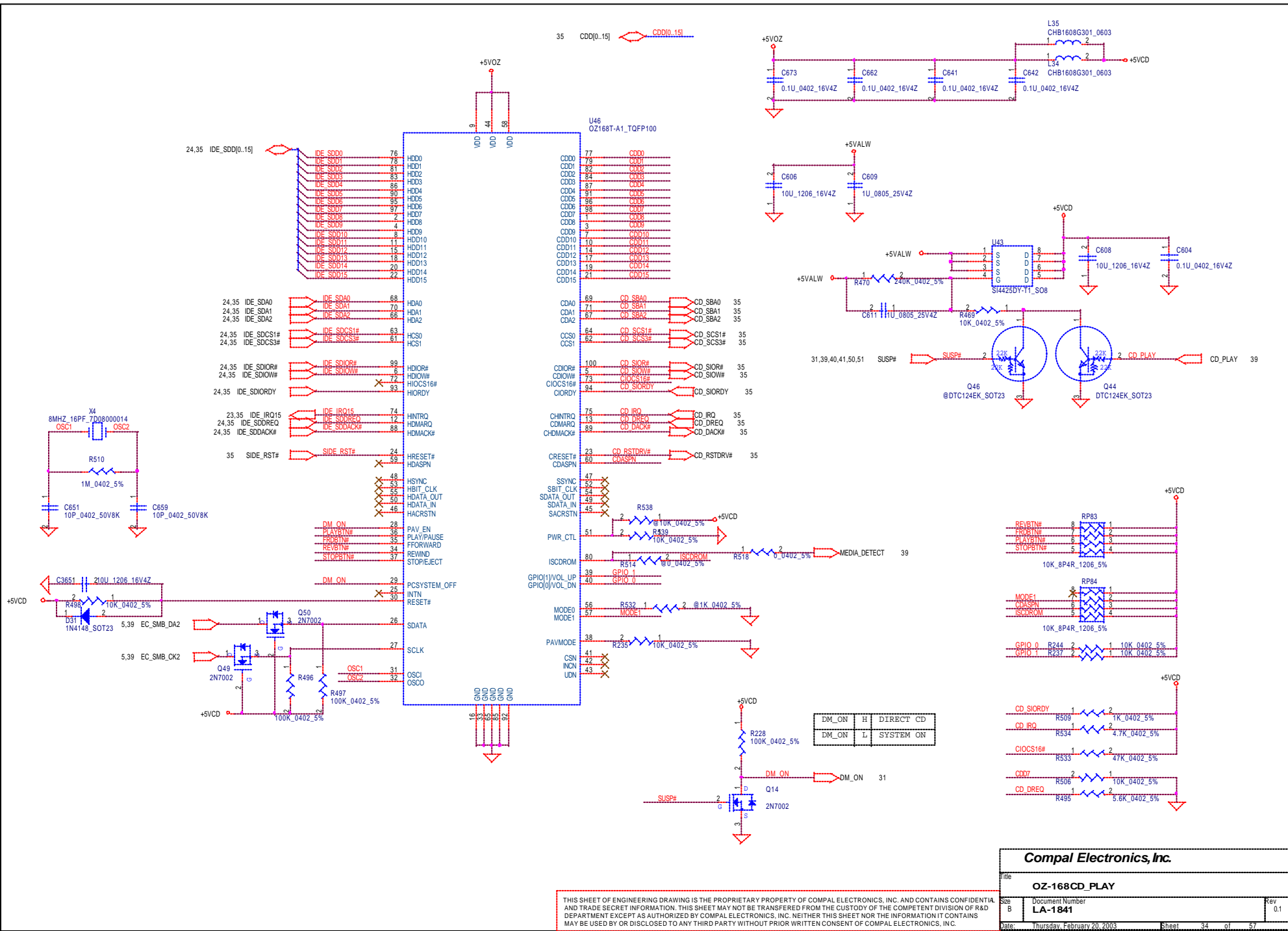


AUDIO Board Conn.



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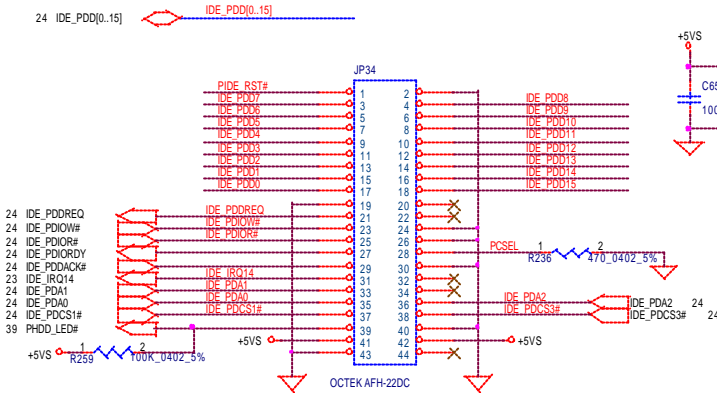
Compal Electronics, Inc.		
Title: AMP & AudioJack		
Size: B	Document Number: LA-1841	Rev: 0.1
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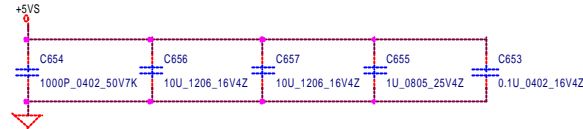
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Compal Electronics, Inc.			
Title			
OZ-168CD_PLAY			
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HDD CONNECTOR



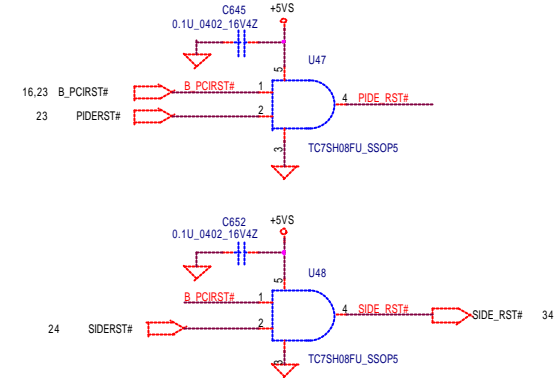
Place caps. near HDD CONN.



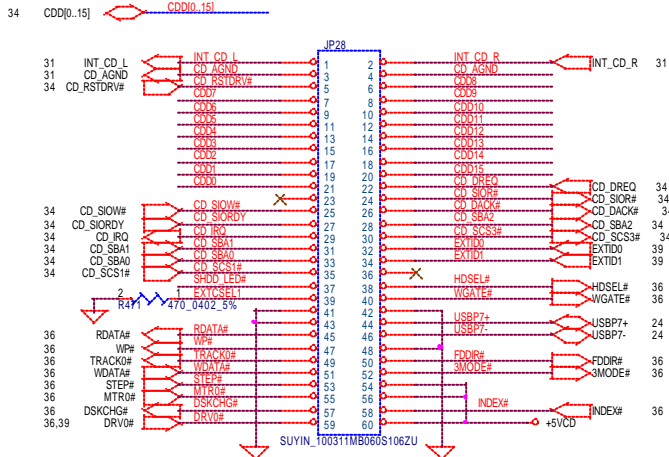
EXTID1	EXTID0	Module
0	0	CDROM
0	1	FDD
1	0	HDD
1	1	TV Tuner/No Module

EXTID3	EXTID2	Module
0	0	CDROM
0	1	FDD
1	0	HDD
1	1	TV Tuner/No Module

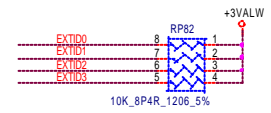
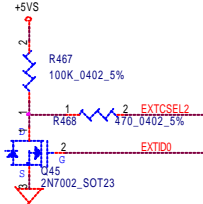
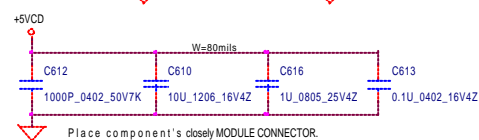
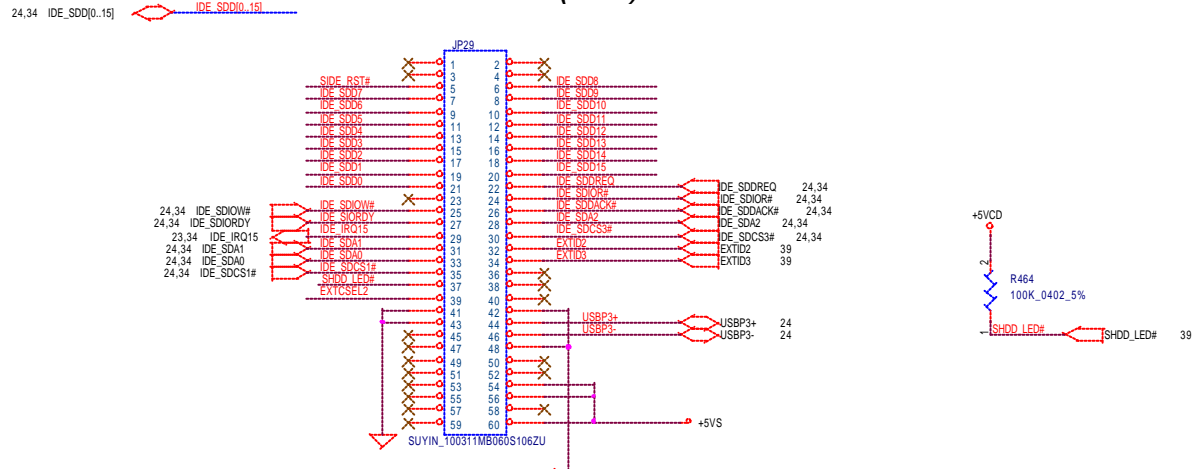
IDE,CD-ROM Module CONN.



Main Module Conn. (Master)



2nd Module Conn. (Slave)



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Compal Electronics, Inc.

Title: **IDE/ FDDMODULECONN.**

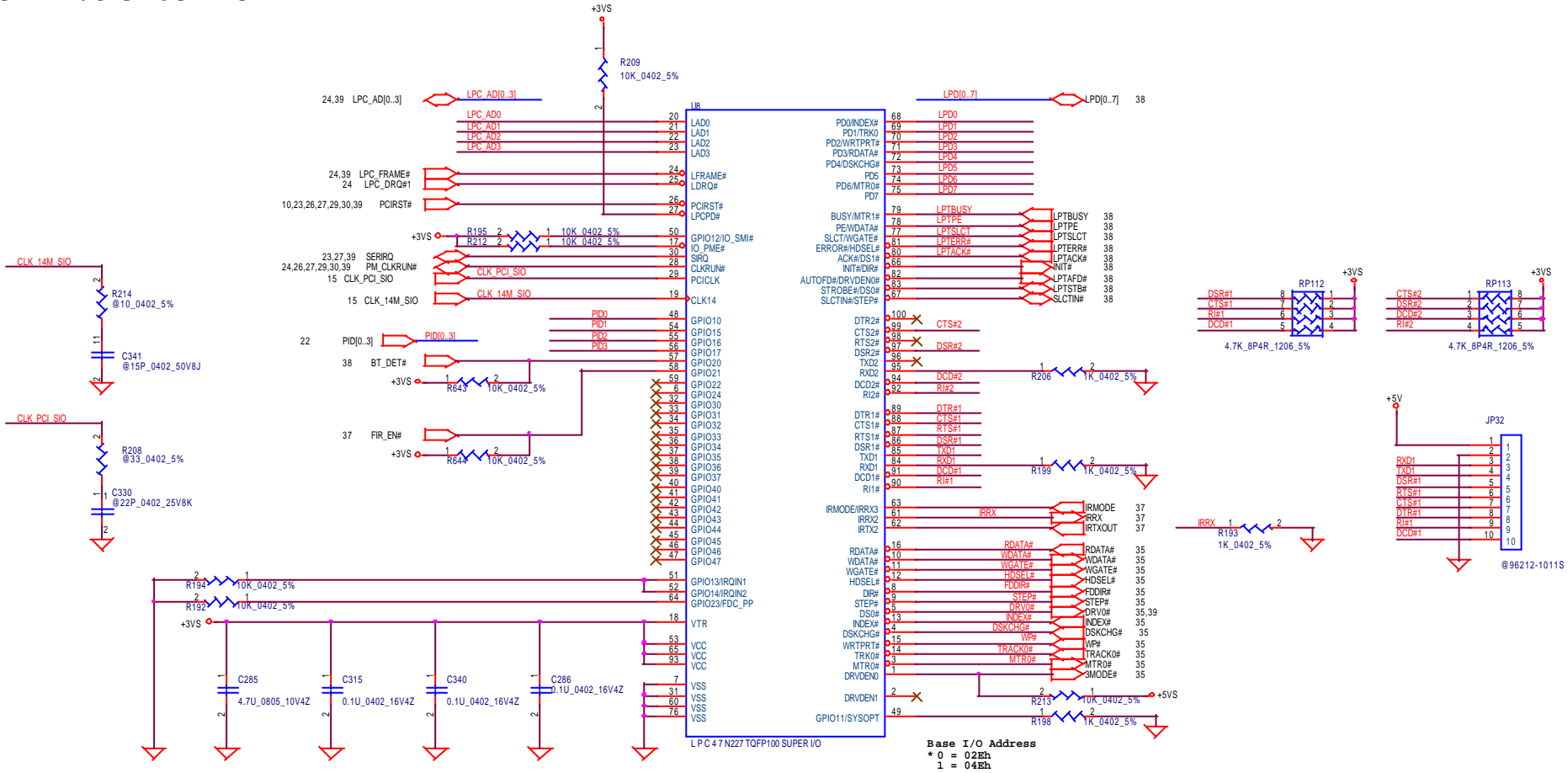
Doc No: **LA-1841**

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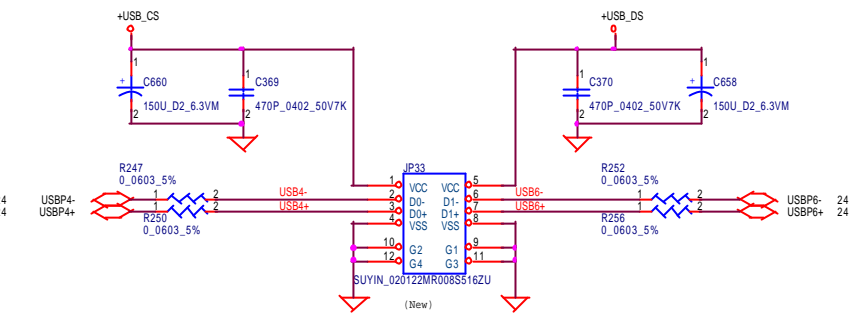
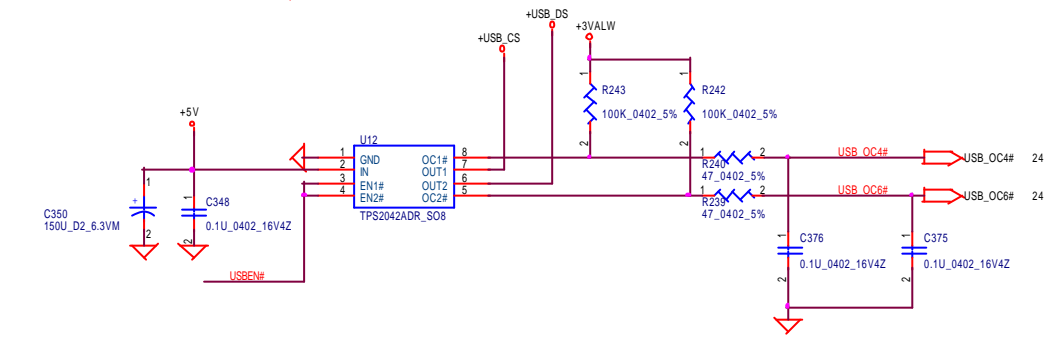
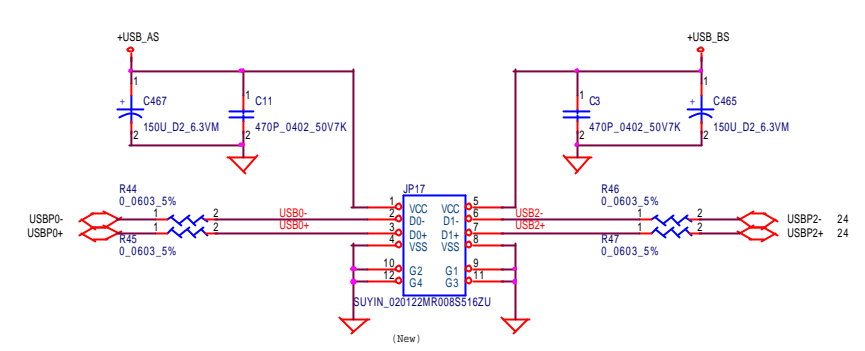
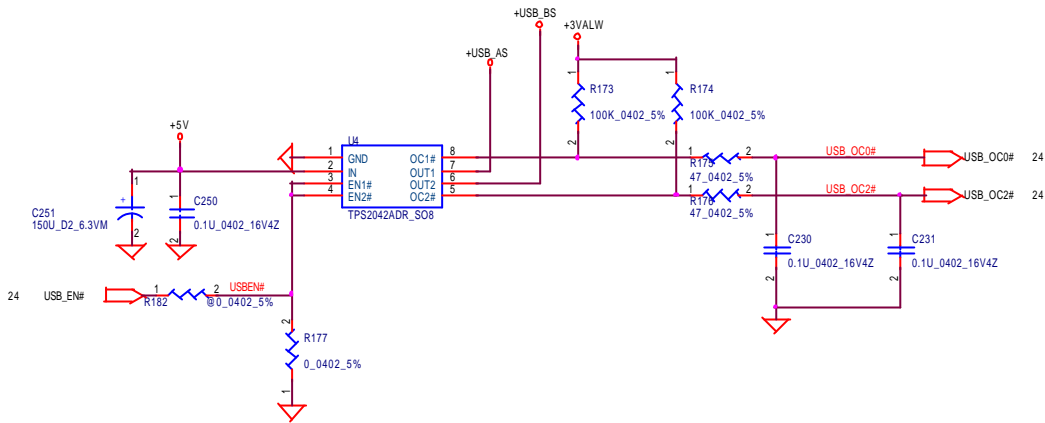
Rev: 0.1

SUPER I/O SMC FDC47N227

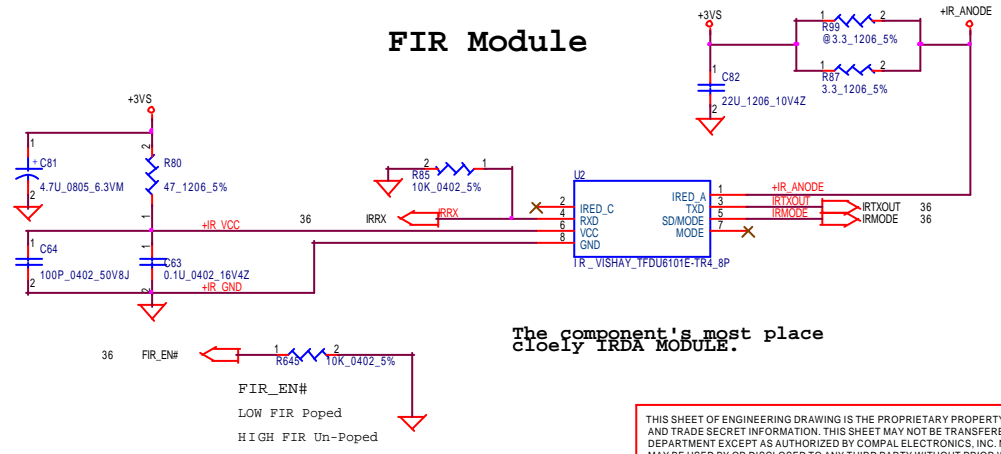


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Compal Electronics, Inc.			
title SUPER I/O			
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FIR Module



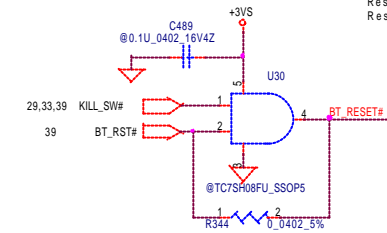
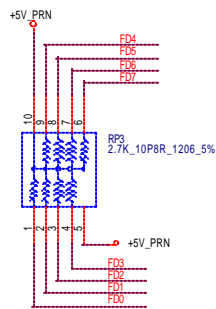
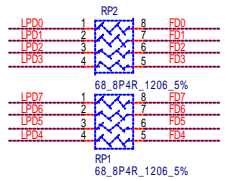
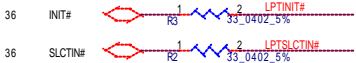
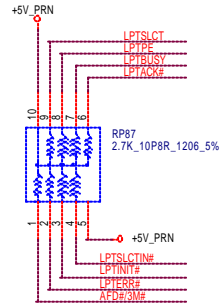
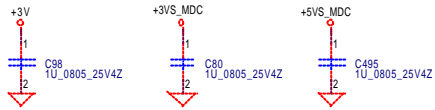
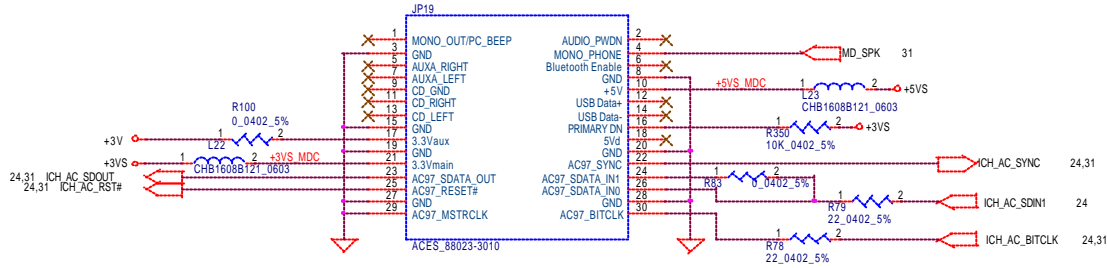
The component's most place closely IRDA MODULE.

FIR_EN#
 LOW FIR Poped
 HIGH FIR Un-Poped

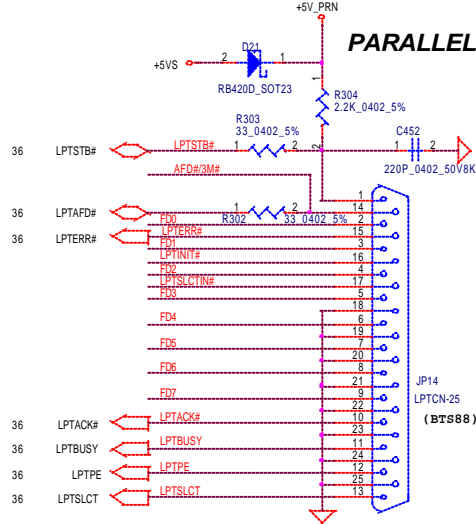
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Compal Electronics, Inc.			
Title			
USB Conn.			
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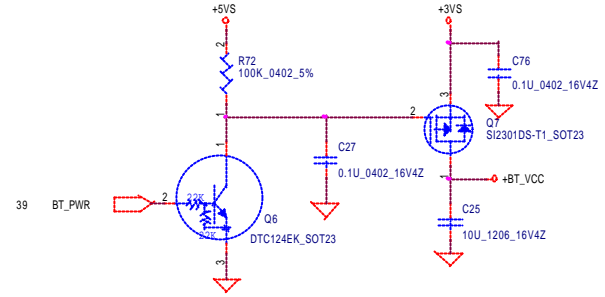
MDC CONN.



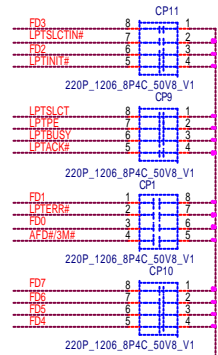
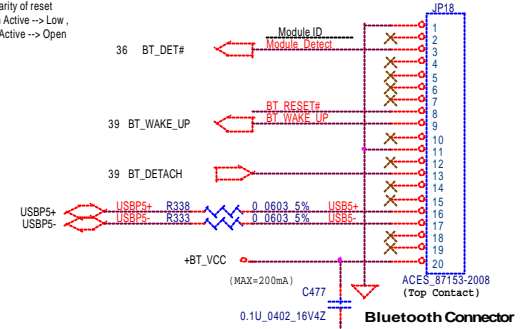
PARALLEL PORT



BlueTooth Interface



Module ID
 Indication for polarity of reset
 Reset input High Active --> Low,
 Reset input Low Active --> Open

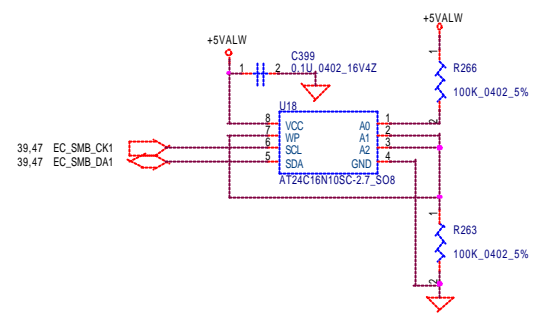
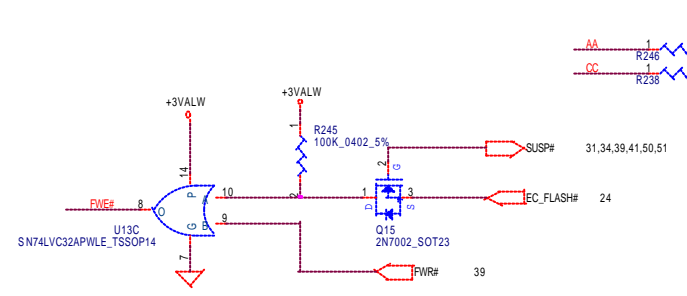
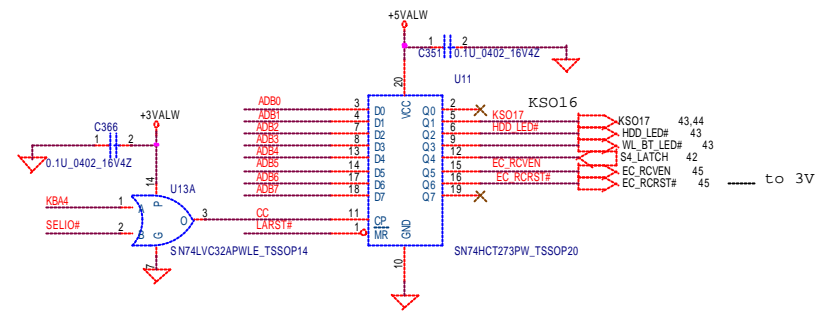
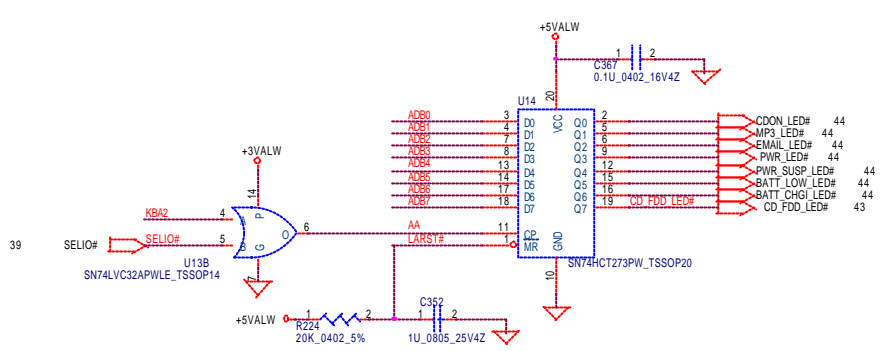


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PARALLELMDCPORT

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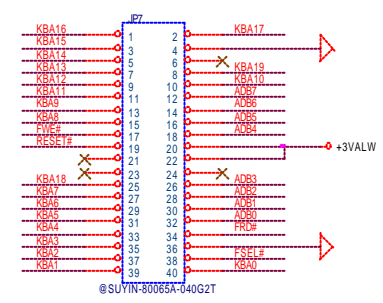
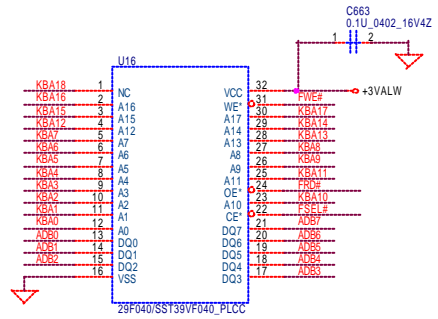
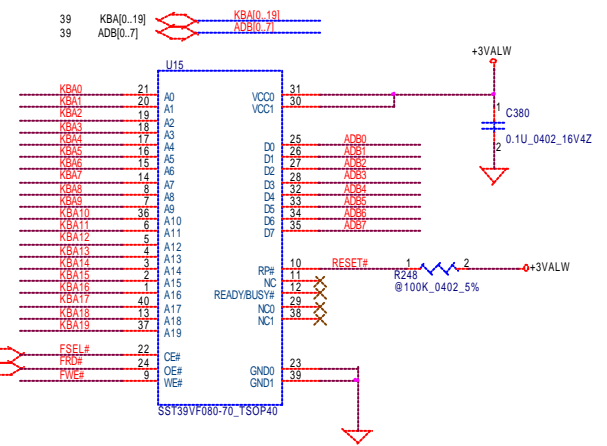
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1MB Flash ROM

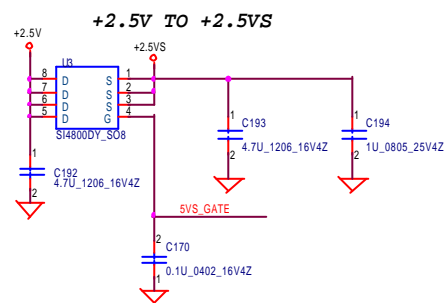
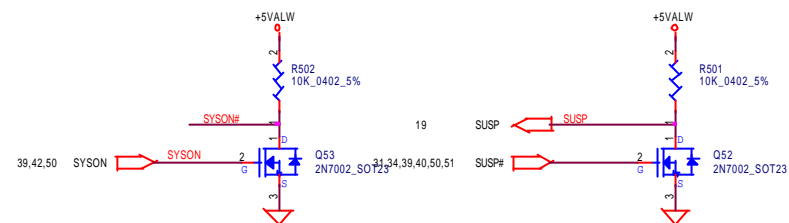
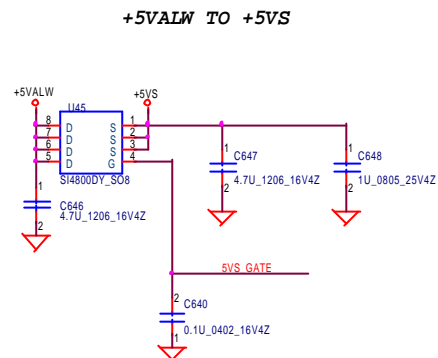
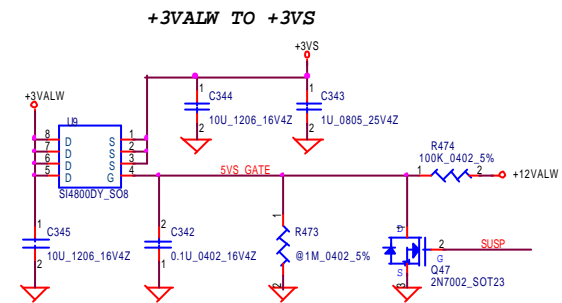
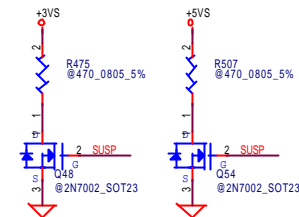
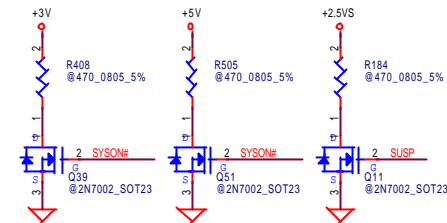
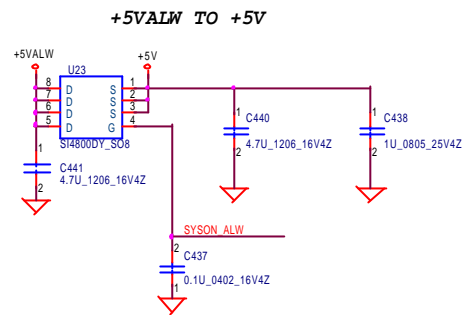
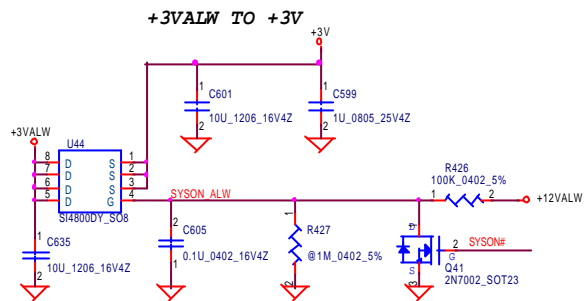
512KB Flash ROM

Flash ROM Socket Conn.



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Compal Electronics, Inc.			
Title			
BIOS & EXT.I/OPORT			
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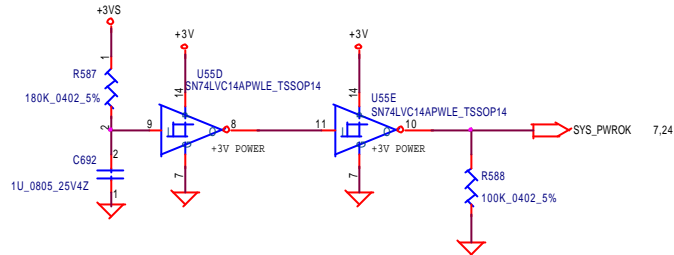


Compal Electronics, Inc.

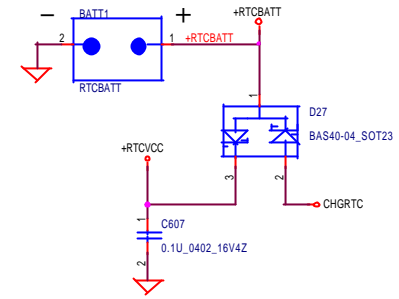
Title		
POWER CONTROLCKT		
Size	Document Number	Rev
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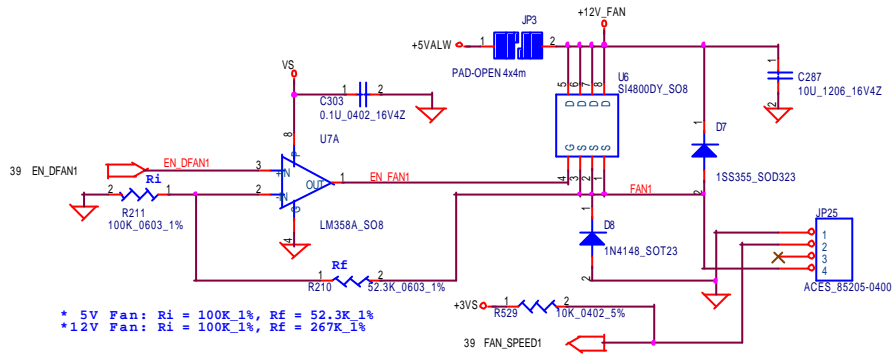
Power ON Circuit



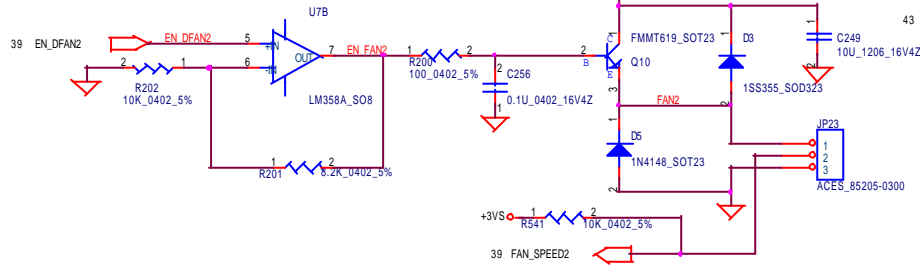
RTC Battery



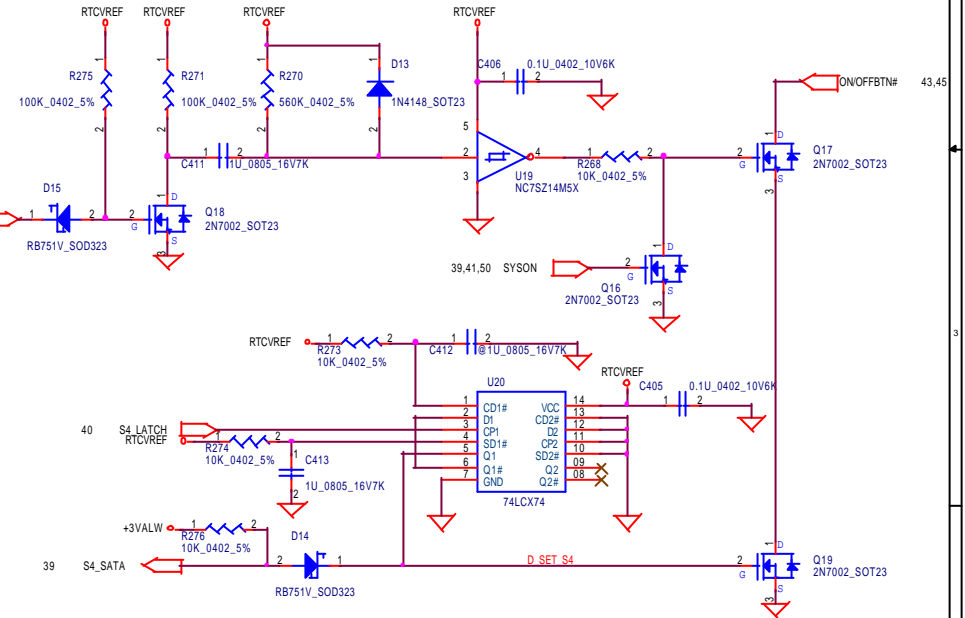
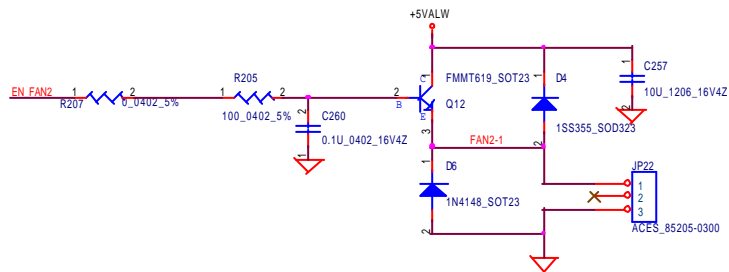
FAN CONN. 1



FAN CONN. 2

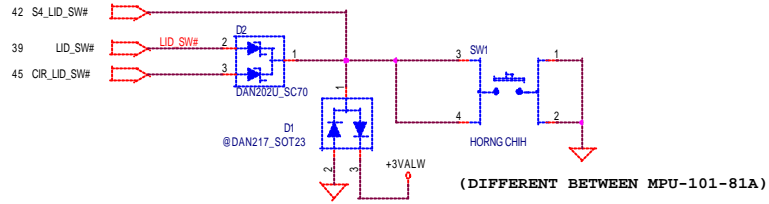


FAN CONN. 3

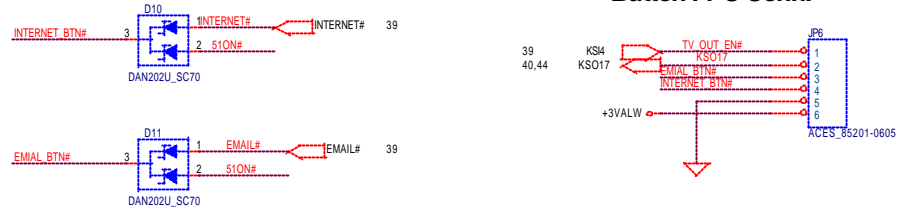


Compal Electronics, Inc.		
Title Power OK/Reset/RTC battery/Lid Switch/Int. KB		
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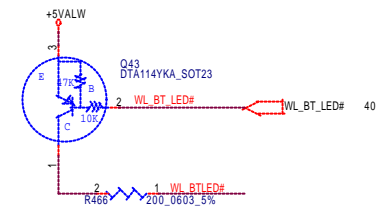
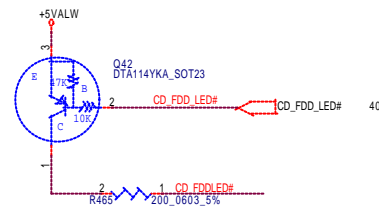
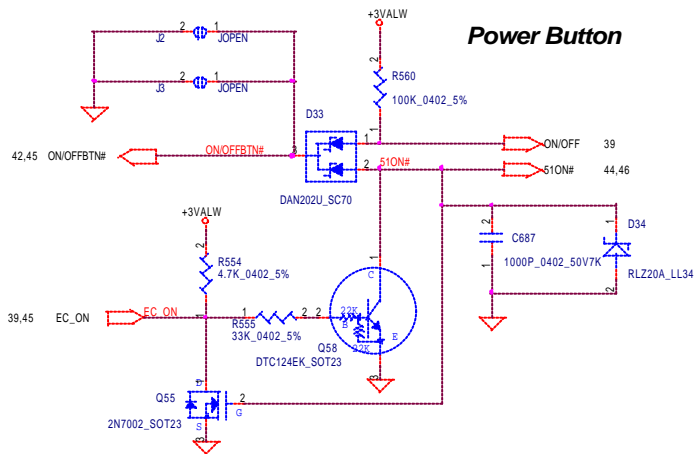
LID Switch



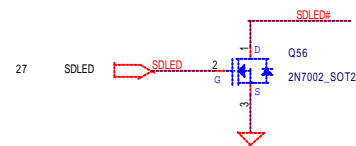
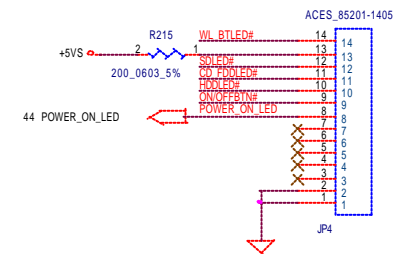
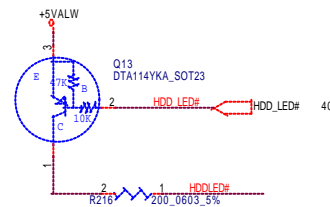
Button FPC Conn.



Power Button

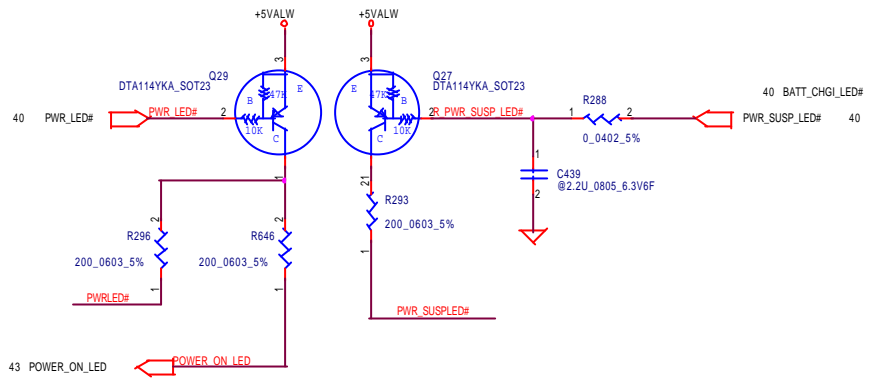


Power FPC Conn.

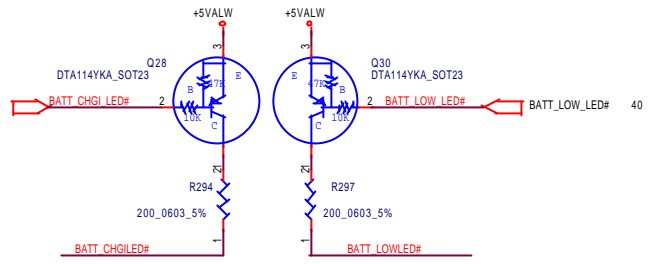


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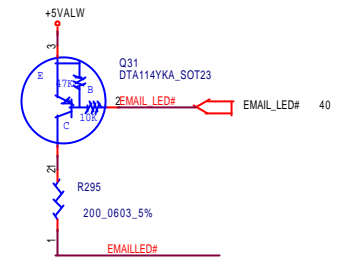
Compal Electronics, Inc.		
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POWER/SUSP LED

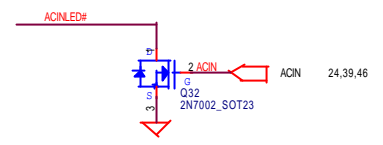
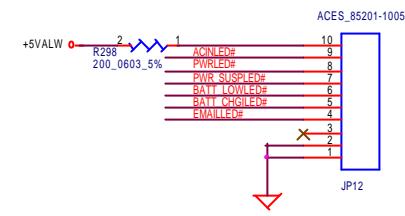


BATTERY CHGI/LOW LED

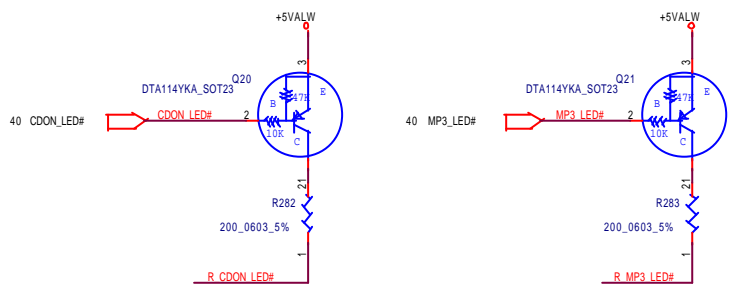


EMAIL LED

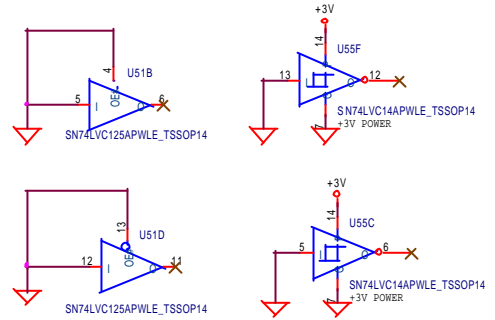
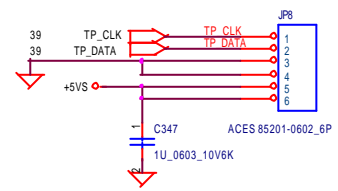
LED FPC Conn.



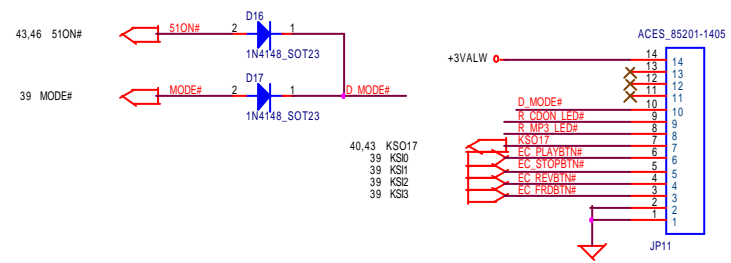
ACIN LED



Touch Pad Connector

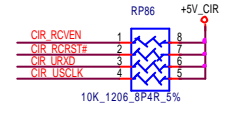
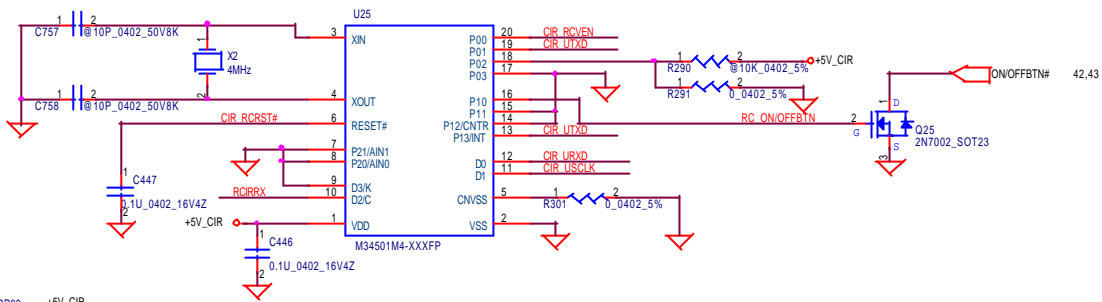
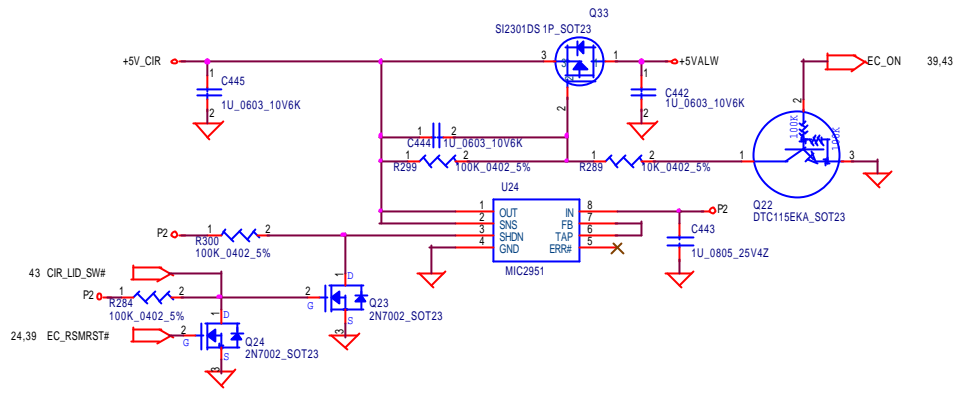
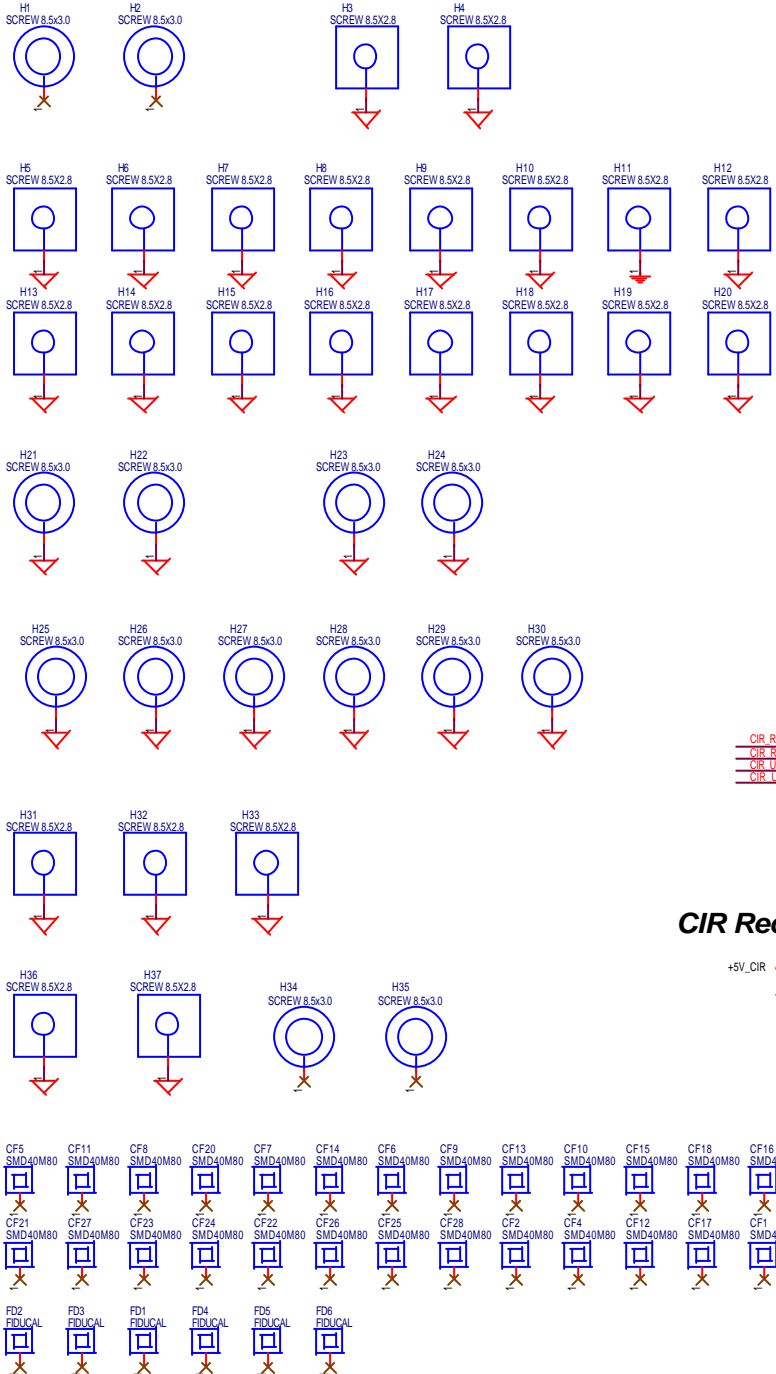


CDPLAY Board Conn.

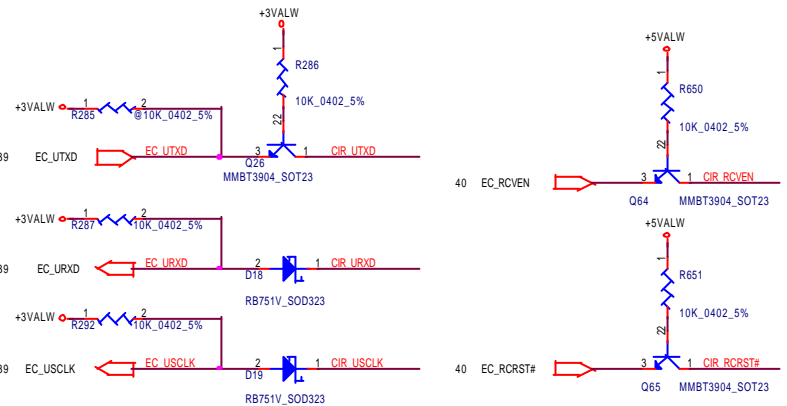
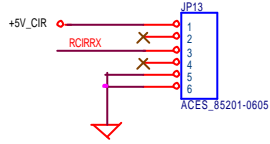


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Compal Electronics, Inc.		
Title Switches & Connectors		
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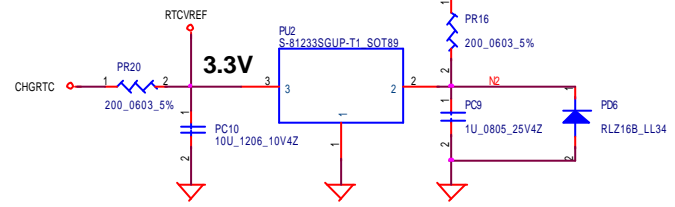
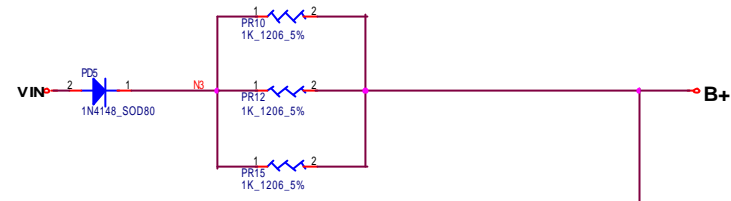
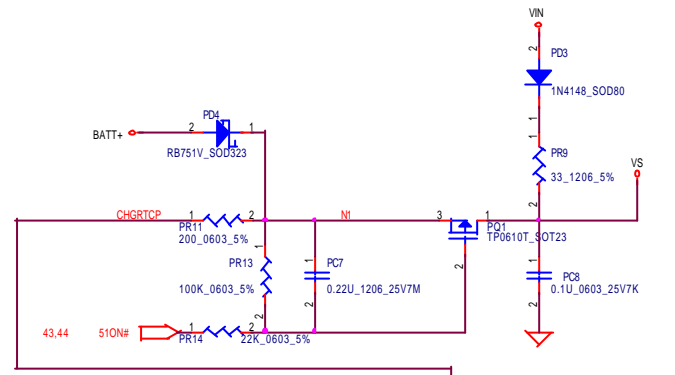
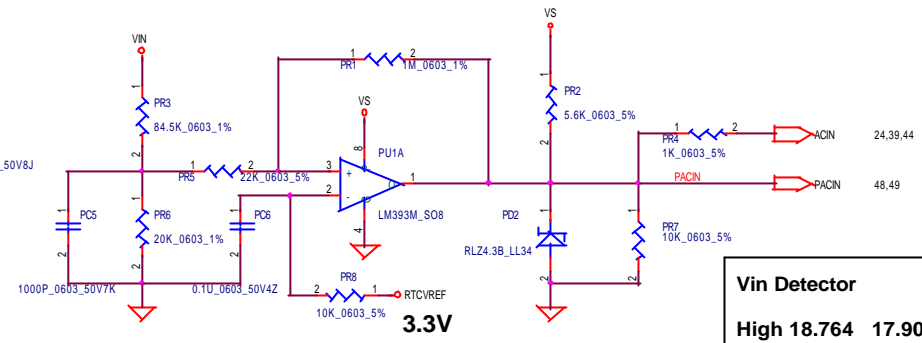
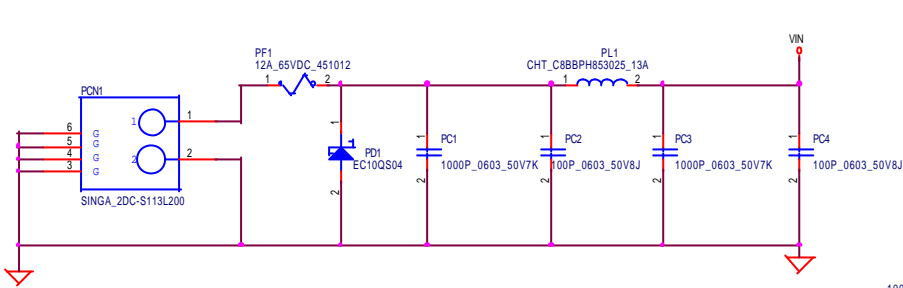


CIR Receiver Board Conn.

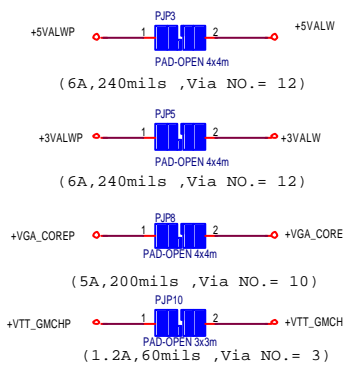
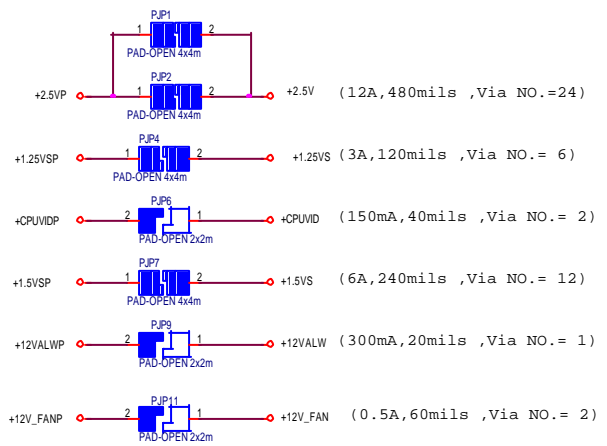
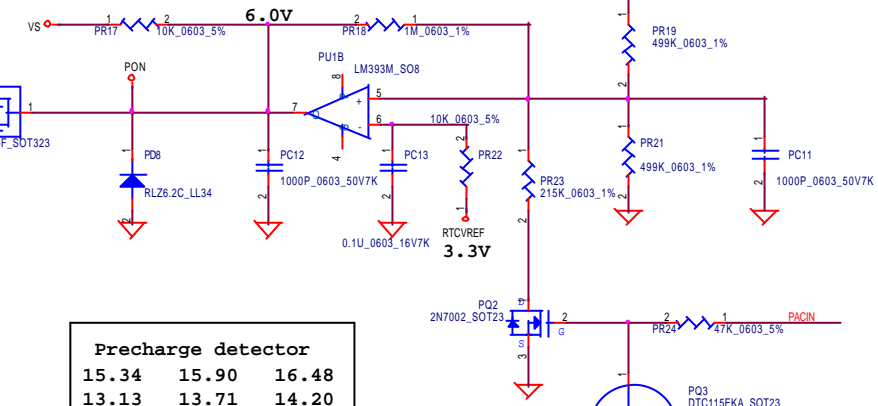


Compal Electronics, Inc.		
Title	CIR & Screws	
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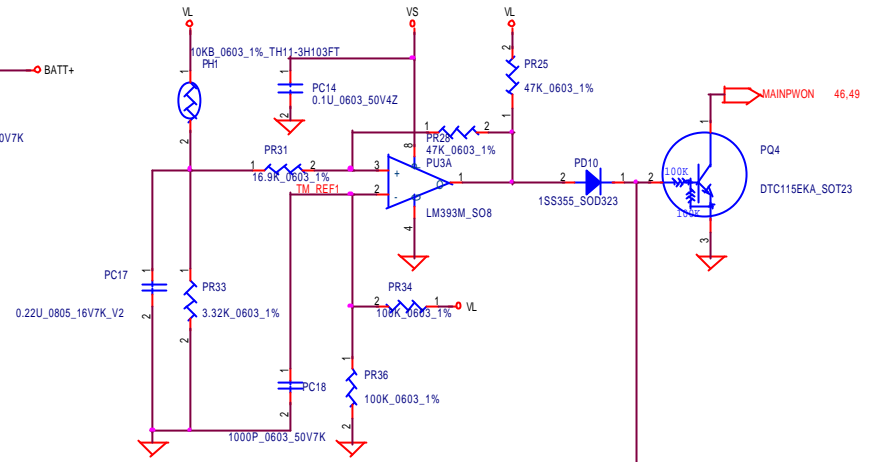
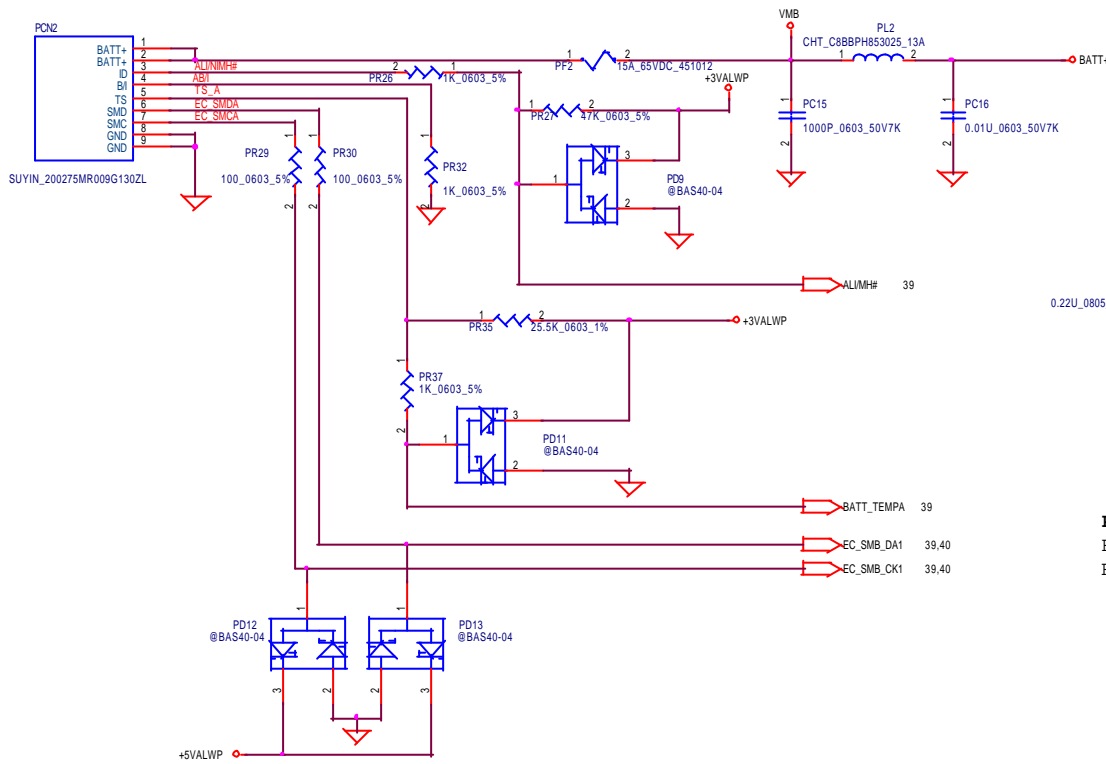
47.49 MAINPWON
48 ACON



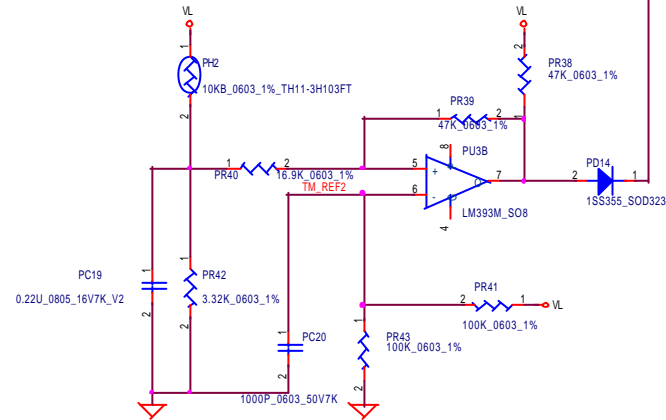
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Compal Electronics, Inc.		
DCIN&DETECTOR		
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PH1 under CPU botten side :
 CPU thermal protection at 84 degree C
 Recovery at 45 degree C

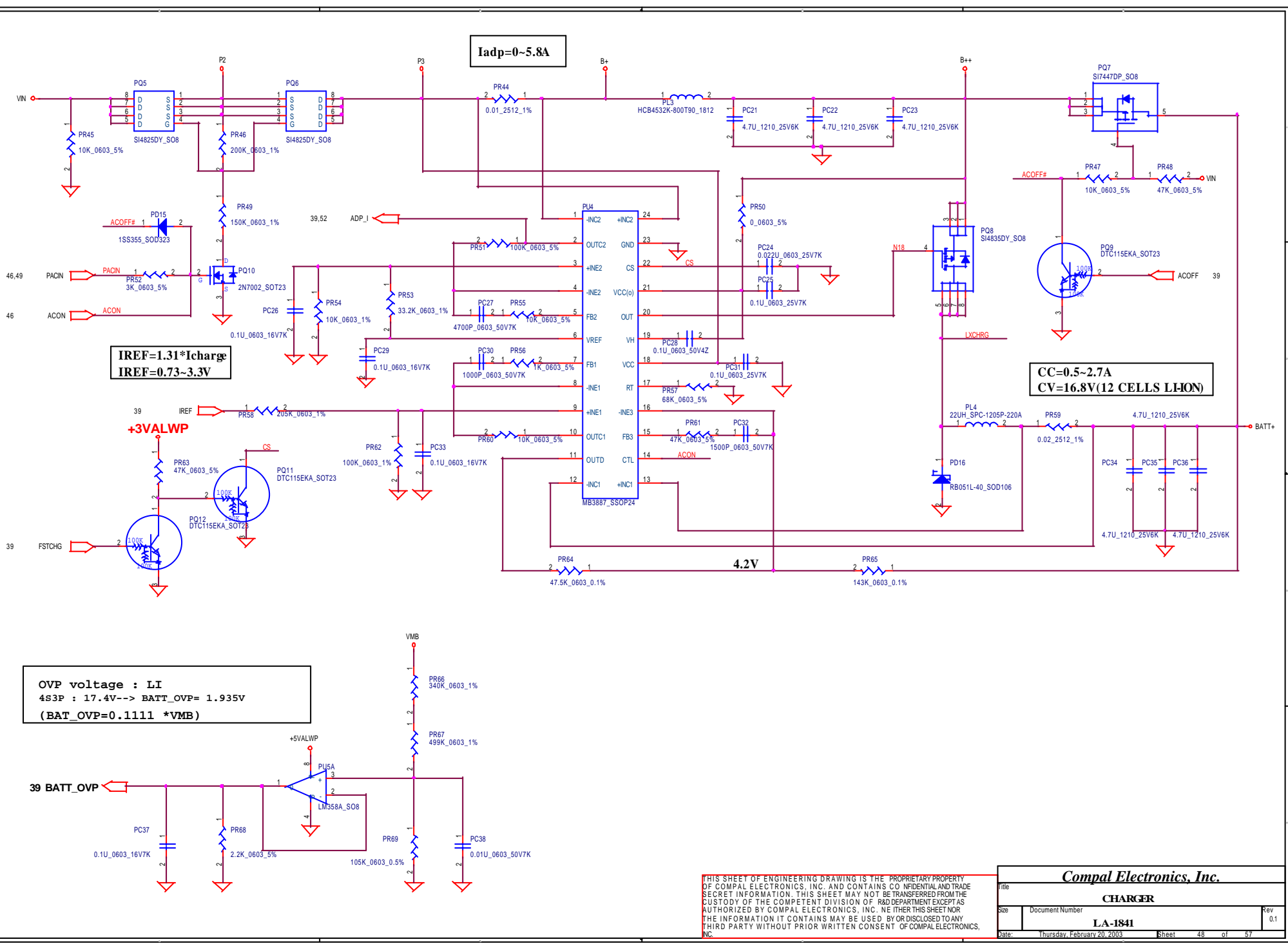


PH2 near main Battery CONN :
 BAT. thermal protection at 84 degree C
 Recovery at 45 degree C



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Compal Electronics, Inc.		
Title BATTERY CONN/OIP		
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I_{adp}=0~5.8A

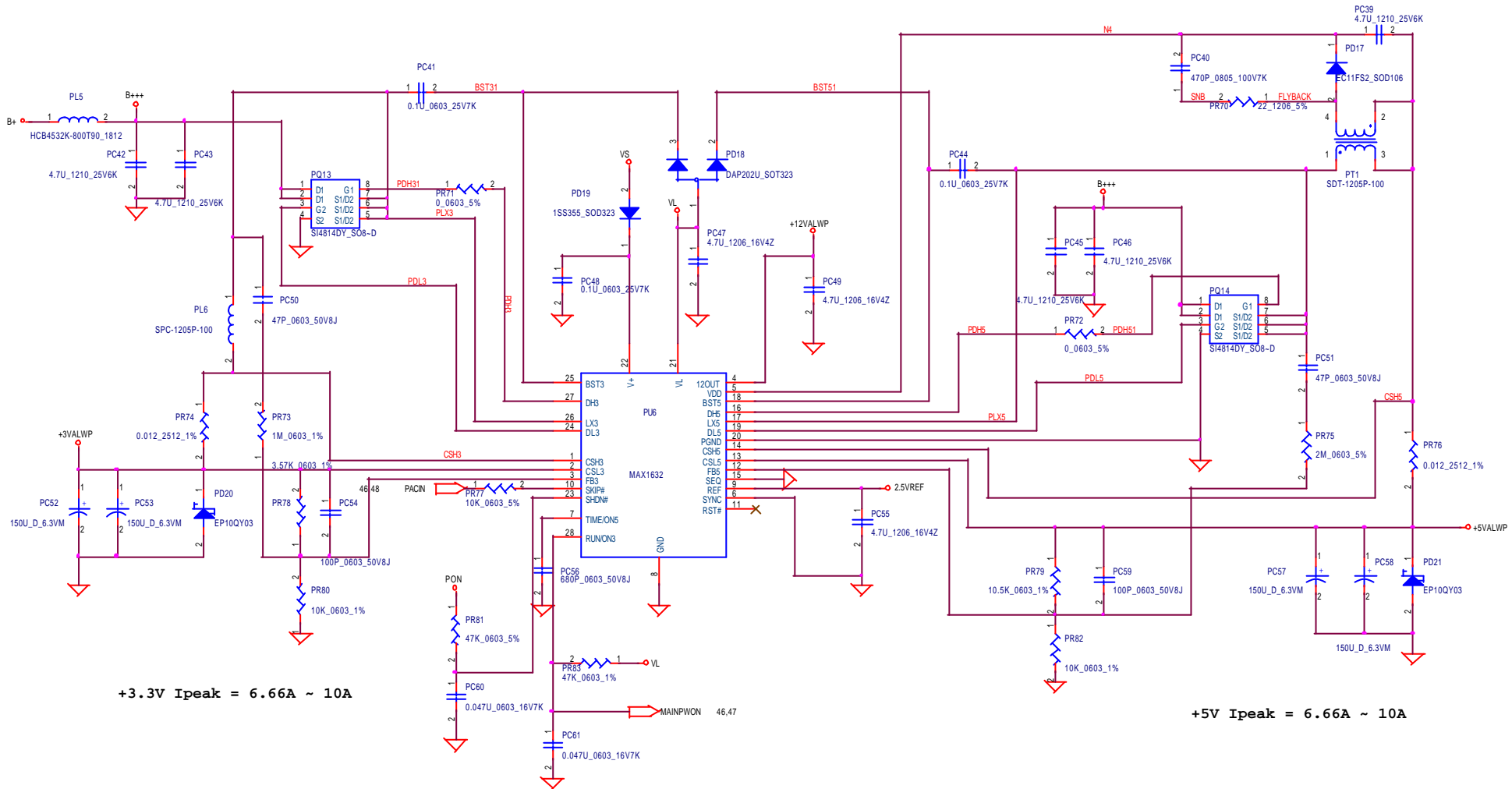
I_{REF}=1.31*I_{charge}
I_{REF}=0.73~3.3V

CC=0.5~2.7A
CV=16.8V(12 CELLS LI-ION)

OVP voltage : LI
4S3P : 17.4V--> BATT_OVP = 1.935V
(BATT_OVP=0.1111 *VMB)

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Compal Electronics, Inc.		
CHARGER		
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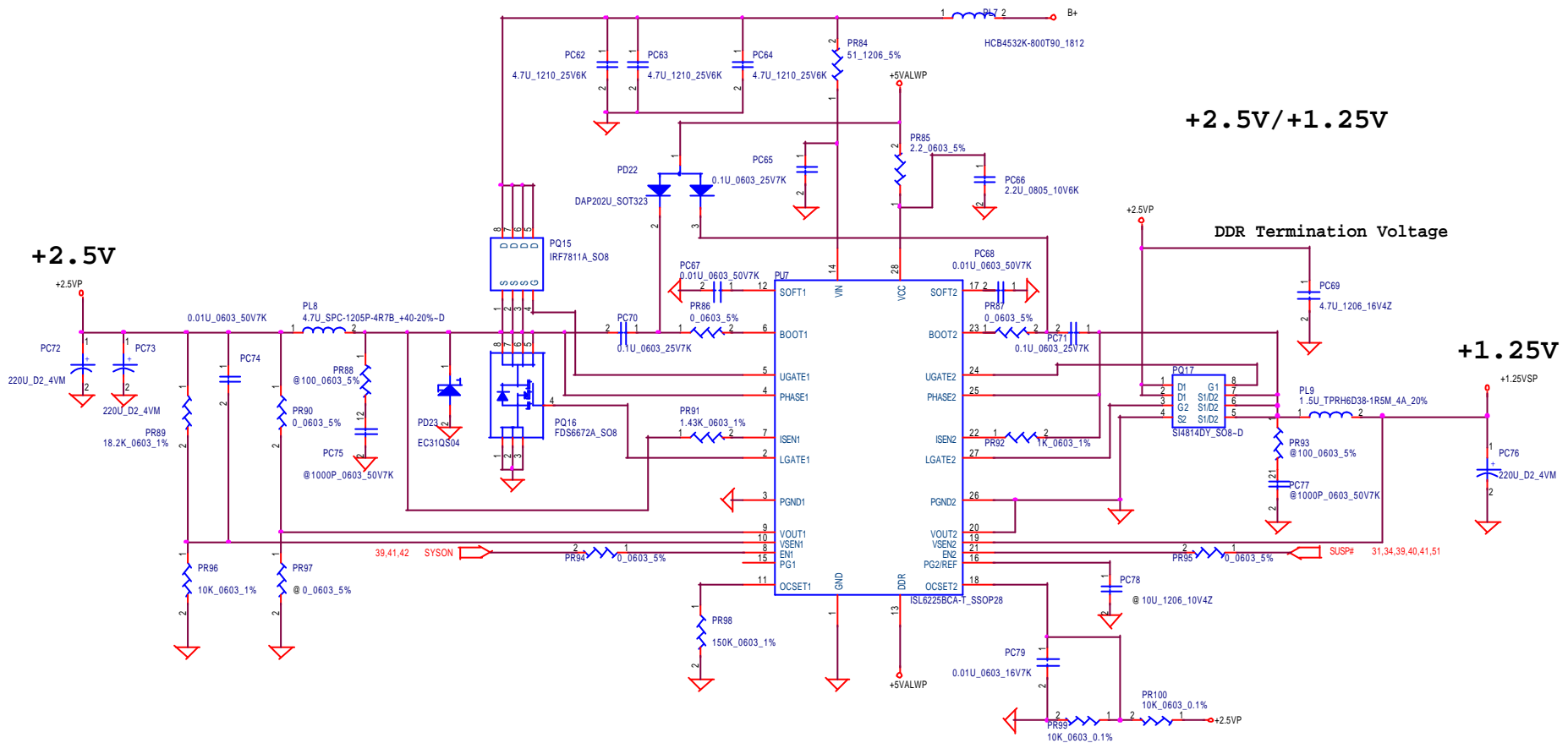


+3.3V Ipeak = 6.66A ~ 10A

+5V Ipeak = 6.66A ~ 10A

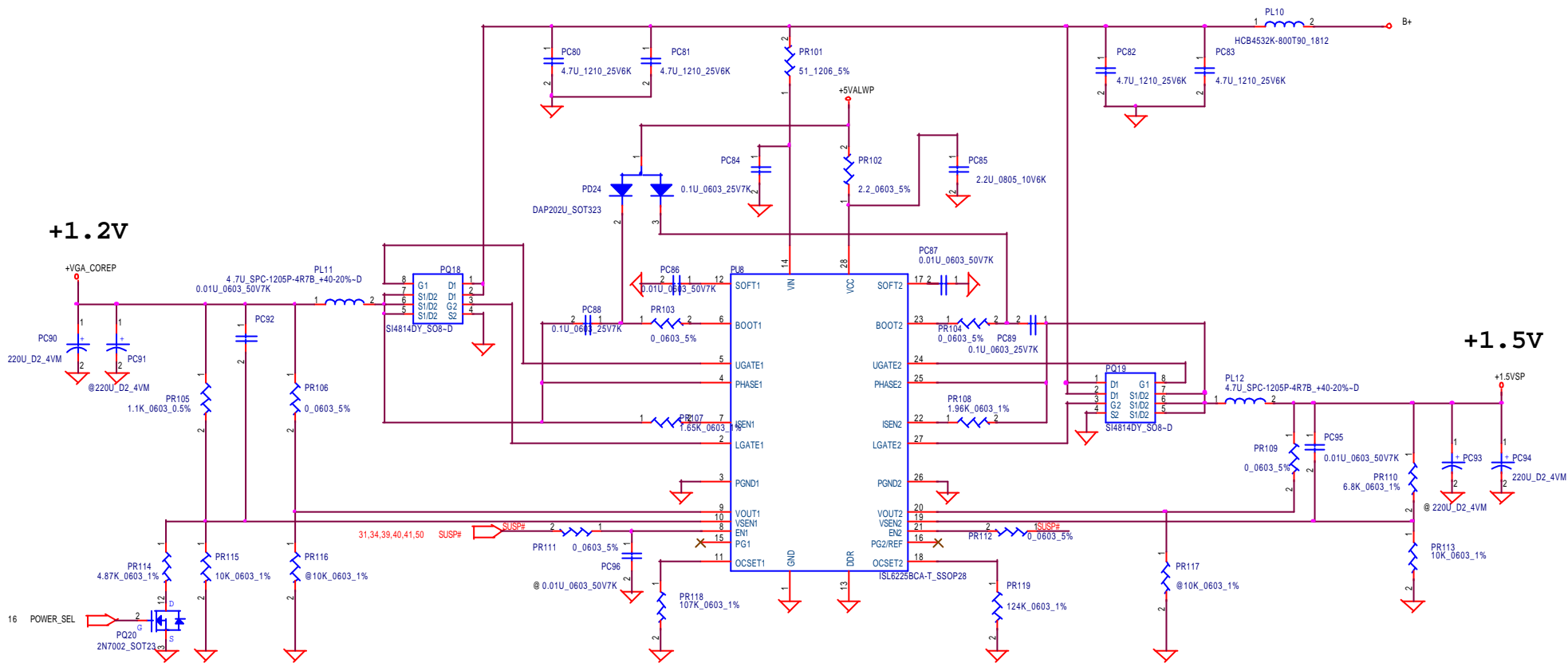
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Compal Electronics, Inc.		
Title 5V/3.3V/12V		
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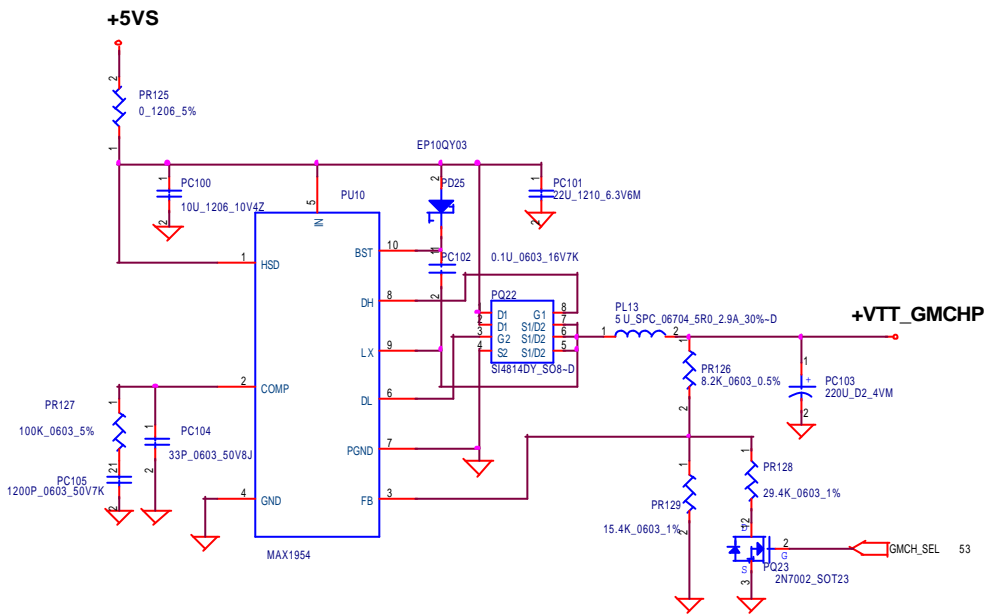
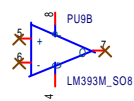
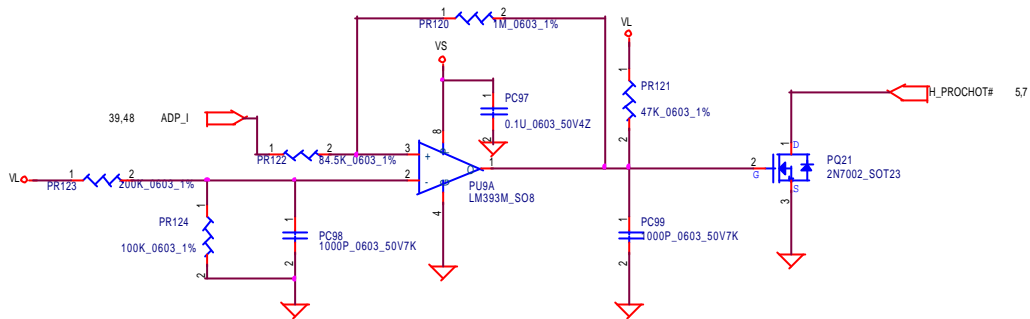
Compal Electronics, Inc.		
Title DDR/2.5V/1.25V		
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	NV18/NV34	NV31
FIX 1.2V	POWER_SEL=1 VOUT=1.2V POWER_SEL=0 VOUT=1.0V	POWER_SEL=1 VOUT=1.0V POWER_SEL=0 VOUT=0.95V
PR105=3.4K_0603_1%	PR105=1.1K_0603_0.5%	PR105=1.1K_0603_0.5%
PR115=10K_0603_1%	PR114=4.87K_0603_1%	PR114=20.5K_0603_1%
UNPOP PR114	PR115=10K_0603_1%	PR115=19.6K_0603_1%
UNPOP PQ20	POP PQ20	POP PQ20

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Compal Electronics, Inc.		
Title VGA_CORE/1.5V		
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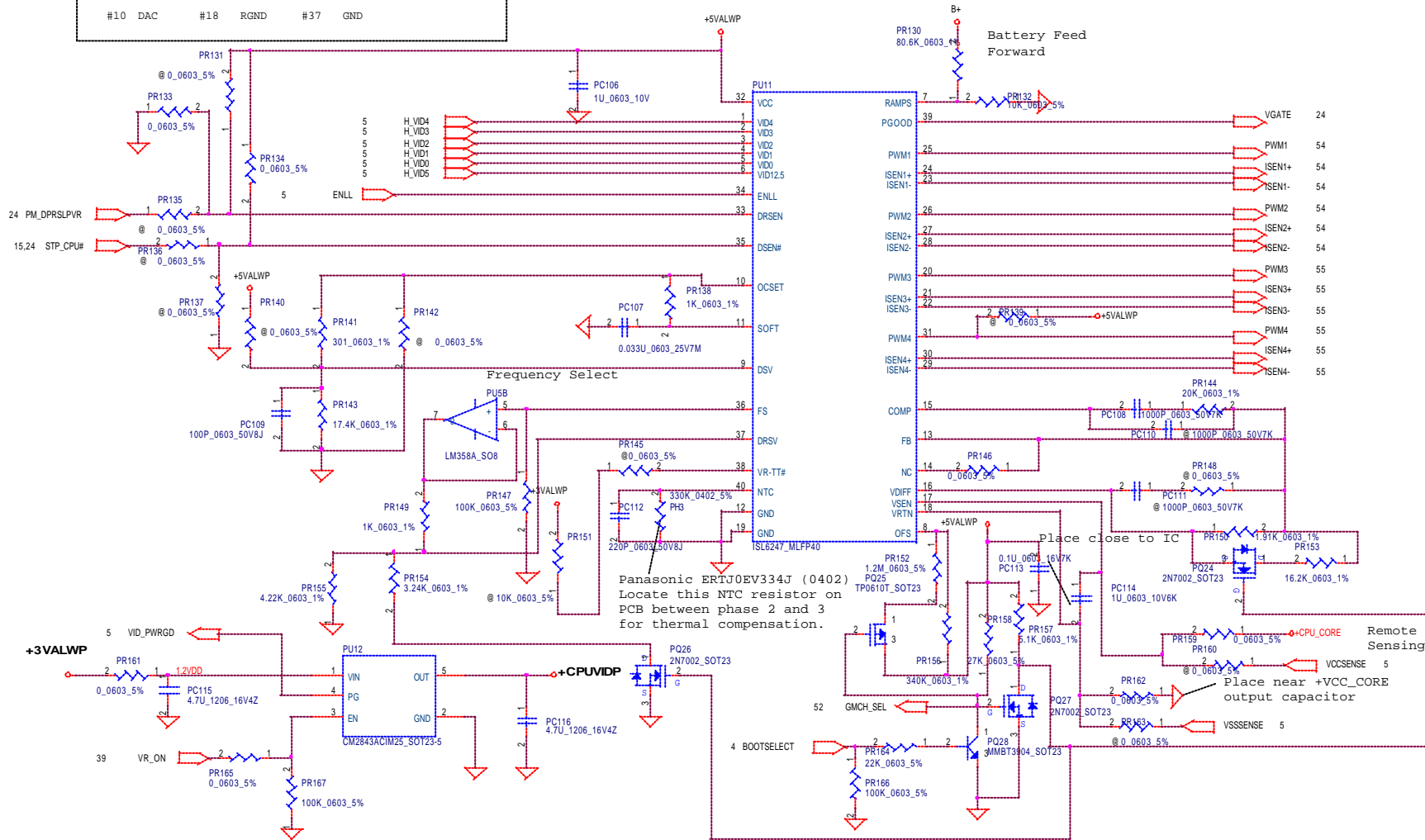
GMCH_SEL=1	VOUT=1.225V FOR PRESCOTT
GMCH_SEL=0	VOUT=1.45V FOR NORTHWOOD

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Compal Electronics, Inc.		
Title VTT_GMCH/CLOCK THROILING		
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Different Pin Definition for ISL6561 in PU9

#7	GND	#11	REF	#33	EN	#38	OVP
#9	TCOMP	#14	IDROOP	#35	GND	#40	GND
#10	DAC	#18	RGND	#37	GND		

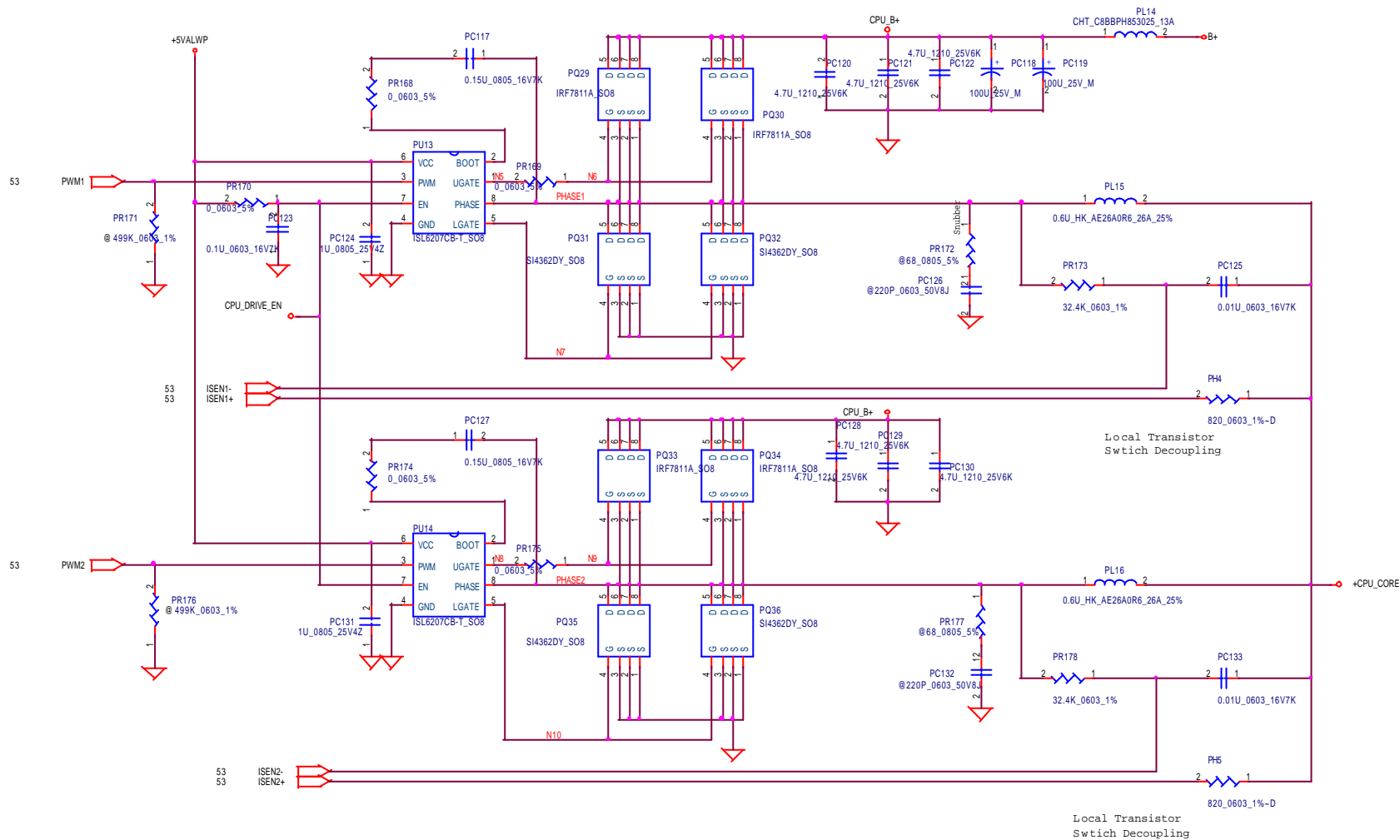


1. When mode control signal is high/ low, the VR will operate to Northwood/ Prescott load line.
2. VID5 (12.5) should be pulled high, when the VR operates to Northwood load line.

BOOTSELECT=1 PRESCOTT
 BOOTSELECT=0 NORTHWOOD

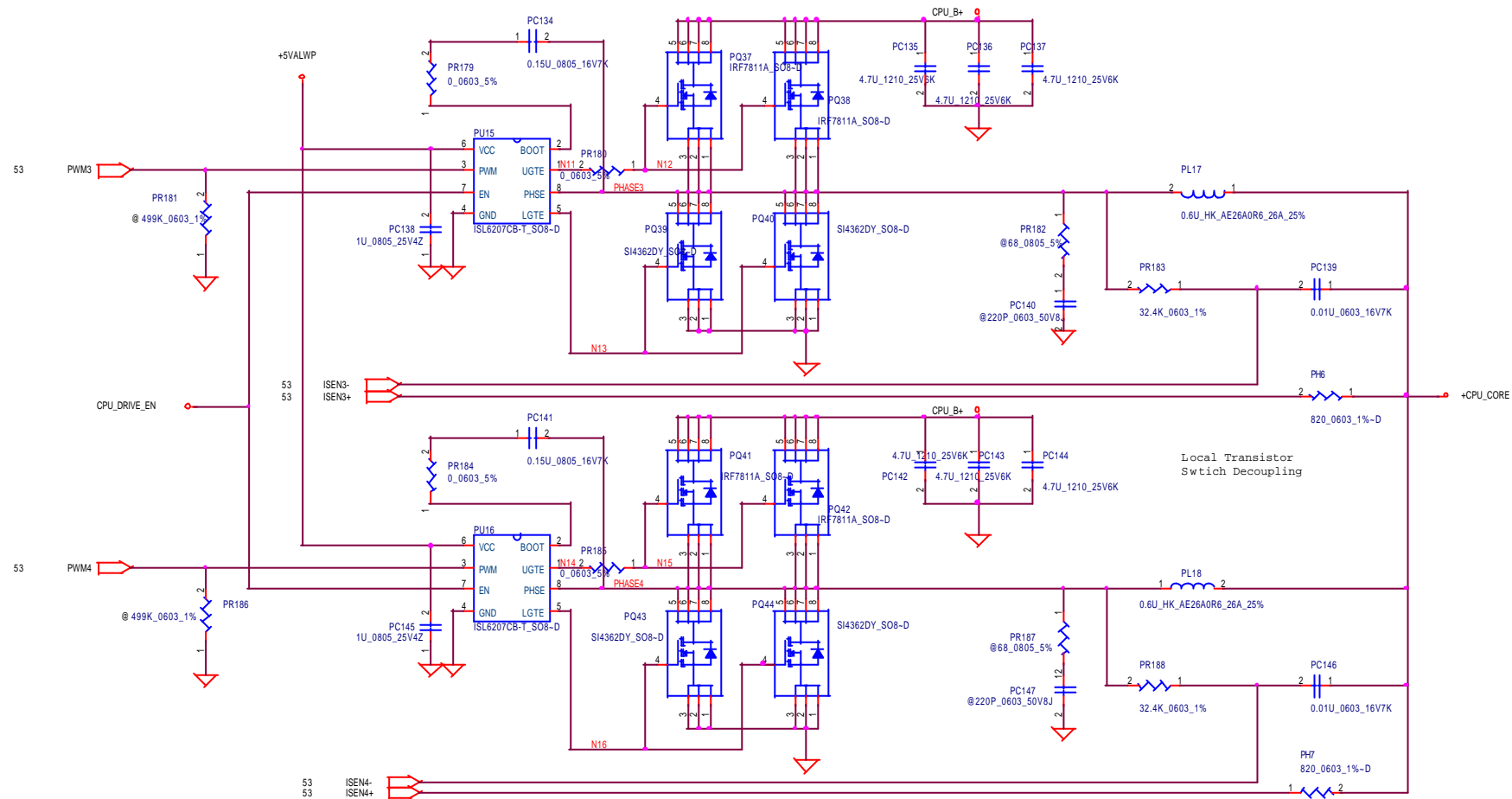
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Compal Electronics, Inc.		
CPU CORE Controller		
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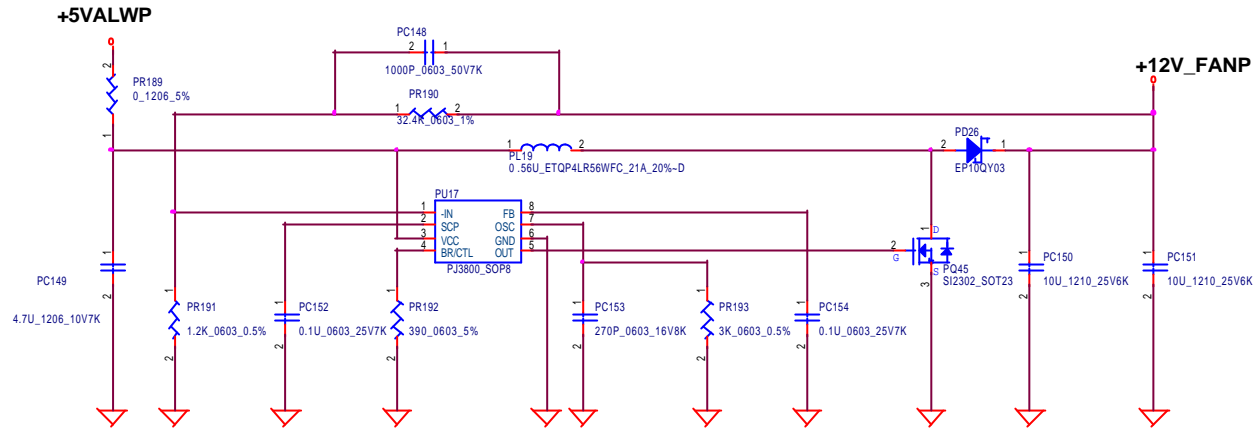
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